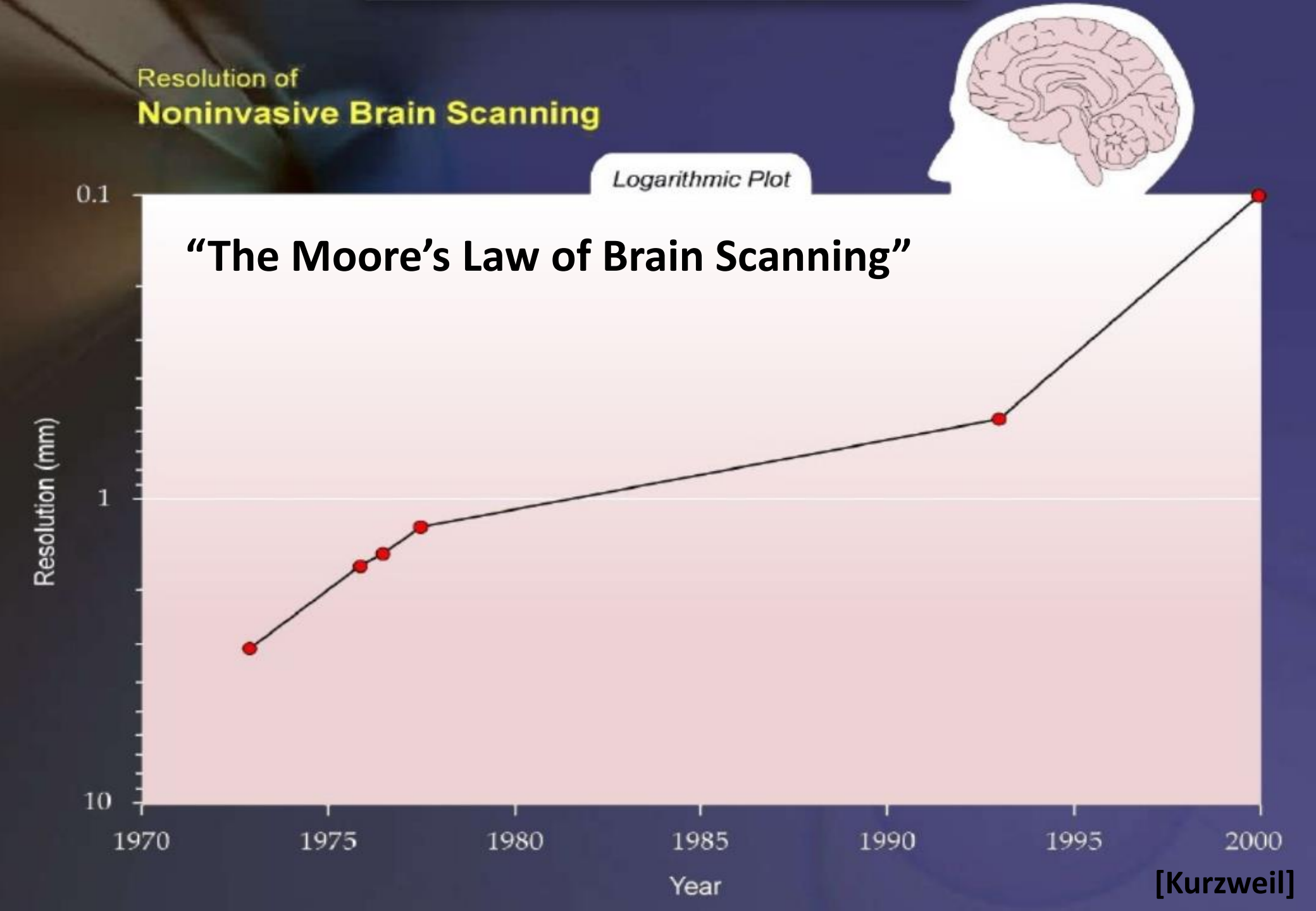
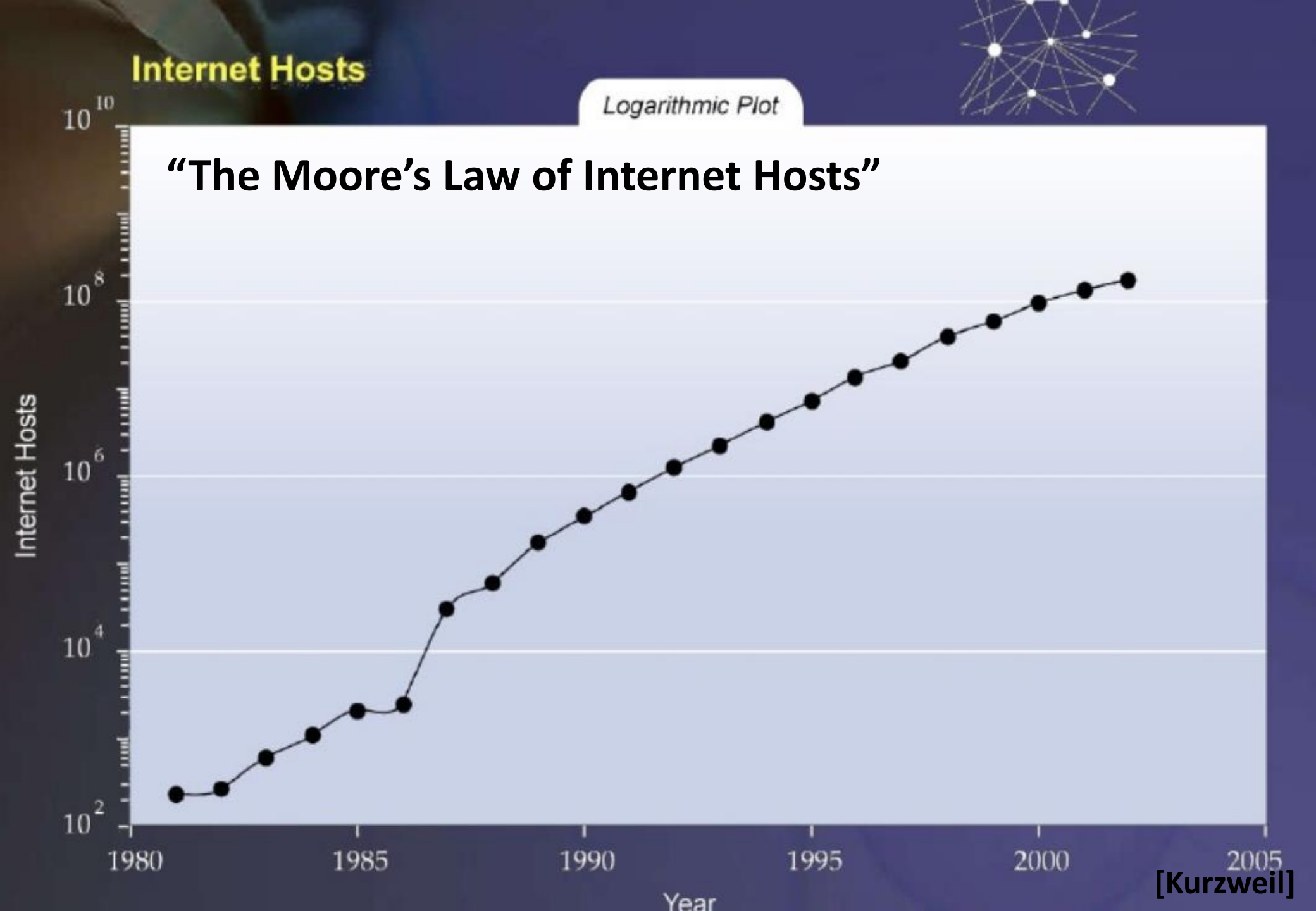
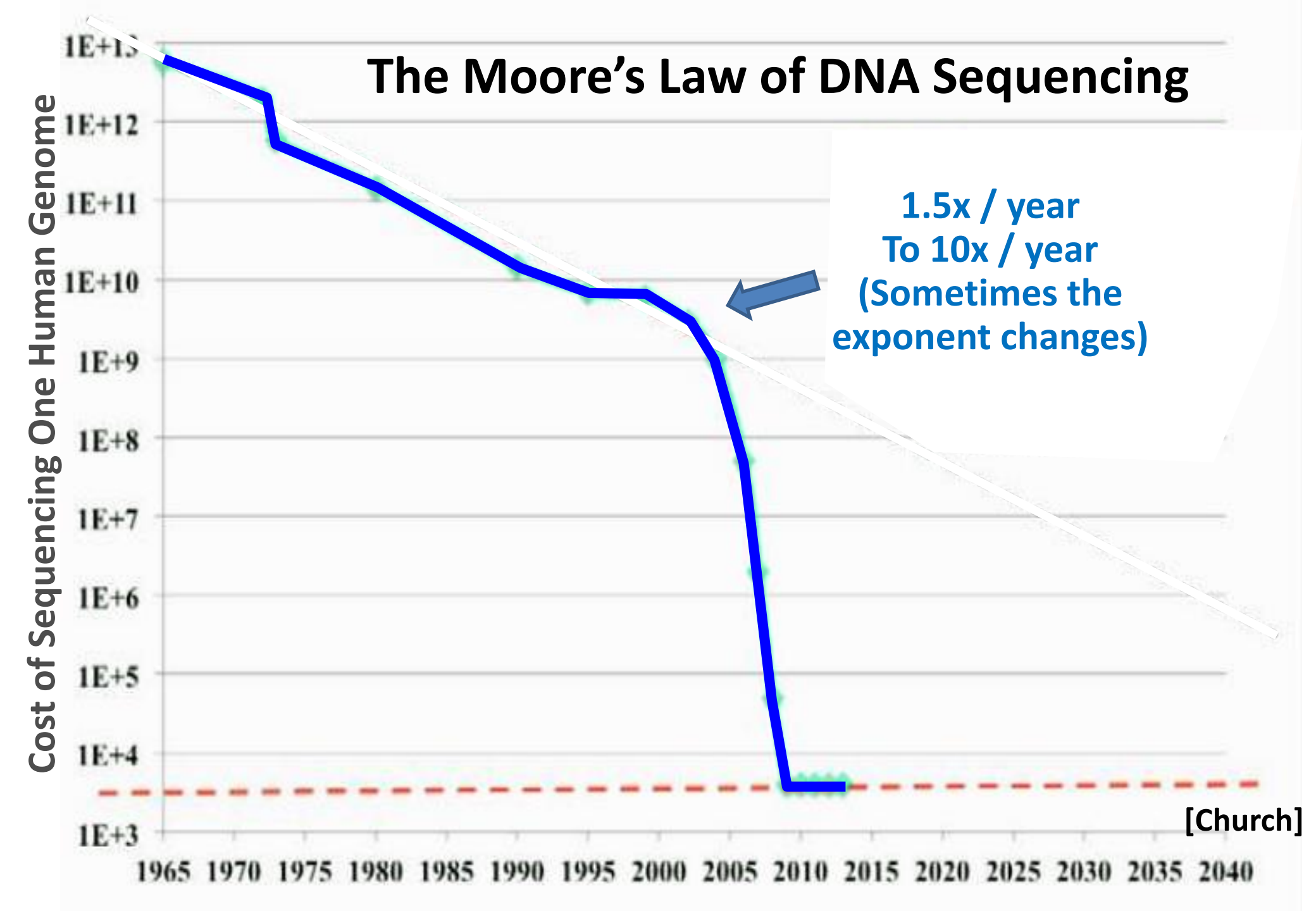
AI Driving Chips, and Chips Driving AI: An Insider's Perspective on Moore's Law

Trent McConaghy
Co-founder & CTO, Solido Design Automation Inc.

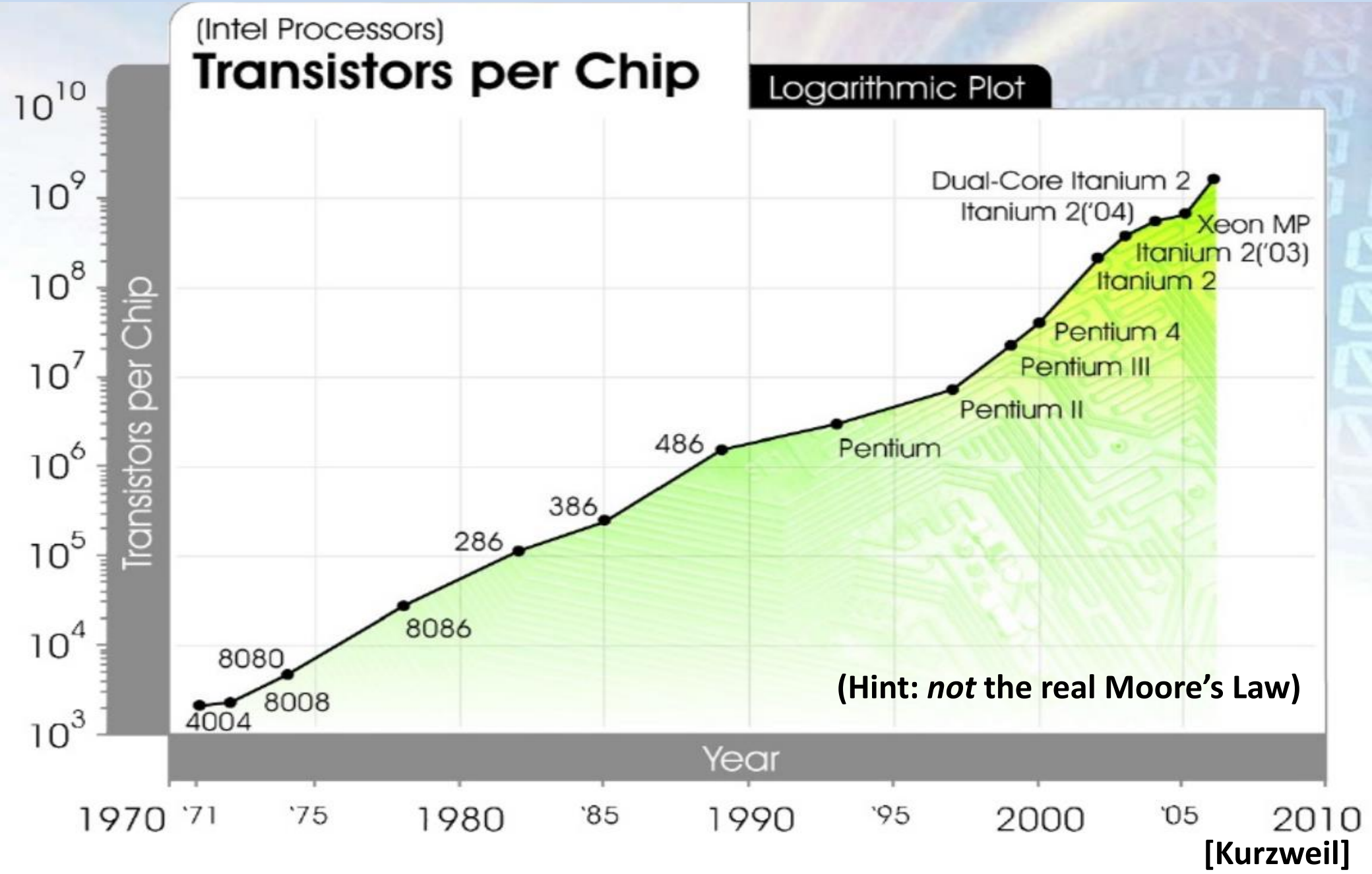
Singularity Meets Self-Improvement
Berlin, October 2013


Resolution of
Noninvasive Brain Scanning
Logarithmic Plot
"The Moore's Law of Brain Scanning"
0.1
1
10
Resolution (mm)
1970
1975
1980
1985
1990
1995
2000
Year
[Kurzweil]


Internet Hosts
Logarithmic Plot
"The Moore's Law of Internet Hosts"
Internet Hosts
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
1980
1985
1990
1995
2000
2005
Year
[Kurzweil]

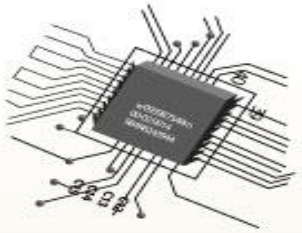

The Moore's Law of DNA Sequencing
Cost of Sequencing One Human Genome
1E+12
1E+11
1E+10
1E+9
1E+8
1E+7
1E+6
1E+5
1E+4
1E+3
1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030 2035 2040
1.5x / year
To 10x / year
(Sometimes the
exponent changes)
[Church]

Will the Real Moore's Law Please Stand Up? (Please stand up)



[Kurzweil]

The Moore's Law of Calculations per $



Calculations per Second per $1,000

10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
1
10^{-2}
10^{-4}
10^{-6}

Electromechanical | *Relay* | *Vacuum Tube* | *Transistor* | *Integrated Circuit*

1900 1910 1920 1930 1940 1950 1960 1970 1980 1990 2000

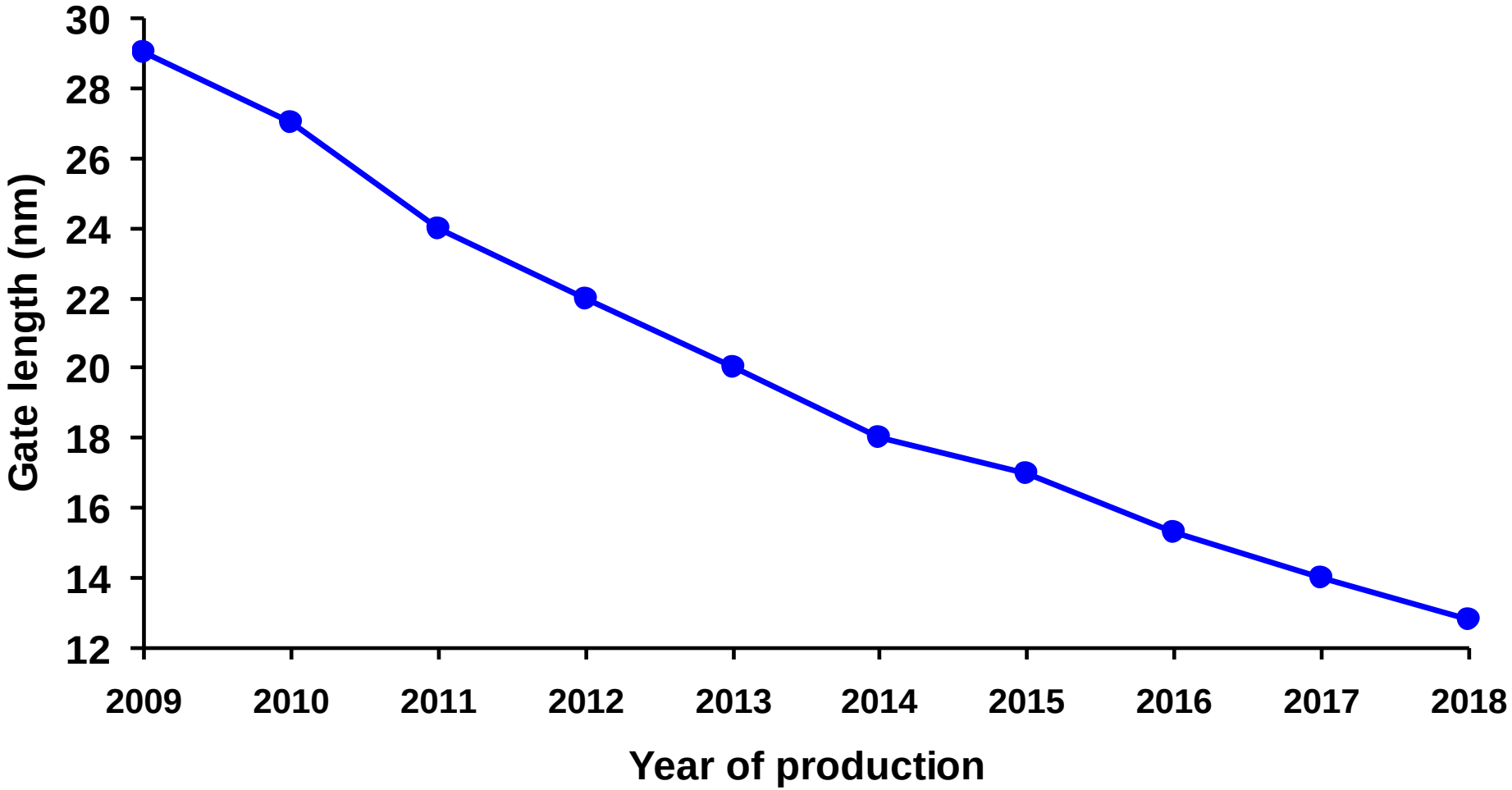
Year

(Hint: *not* the real Moore's Law)

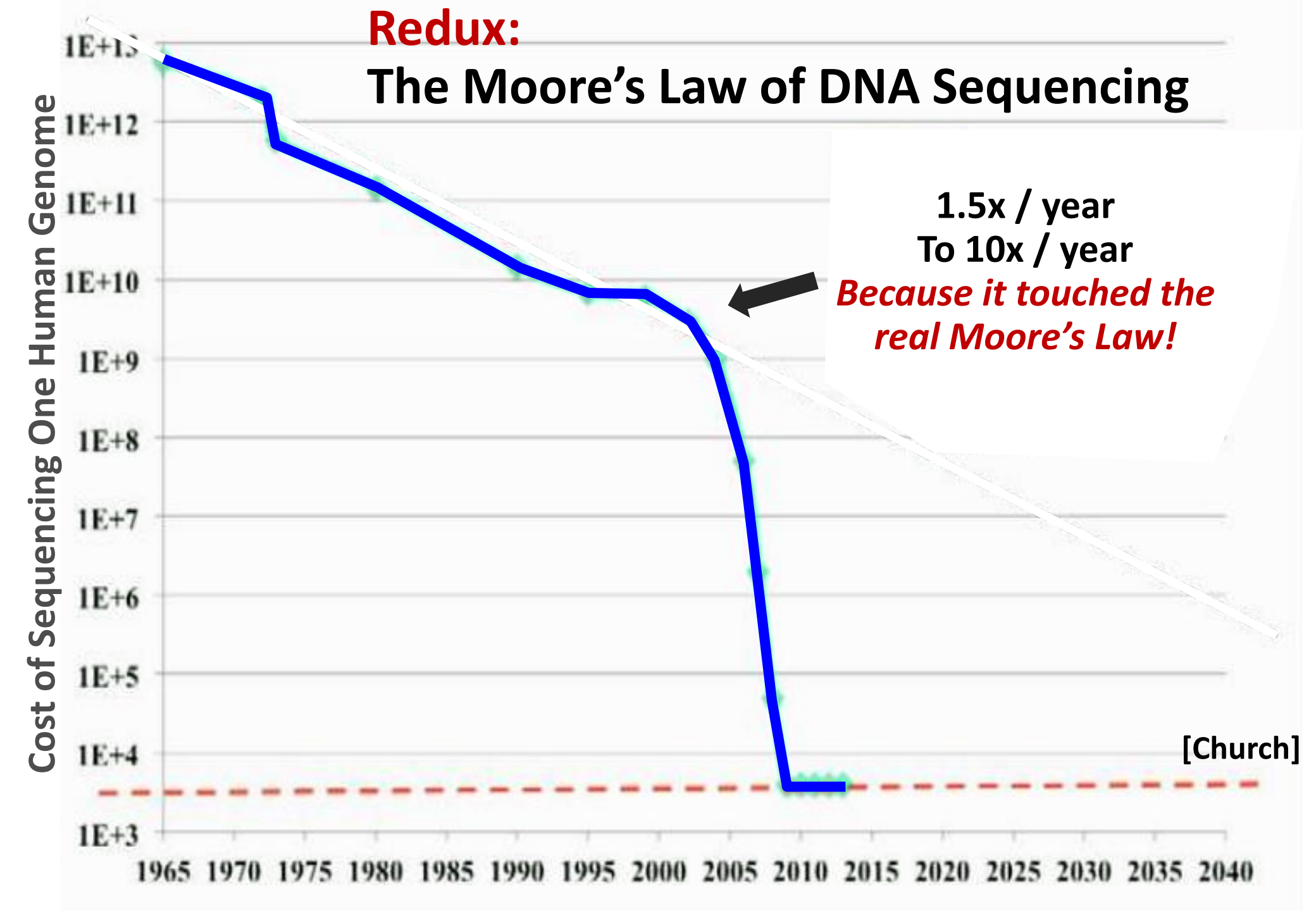
[Kurzweil]

The *Actual* Moore's Law

(About *transistor size*.)

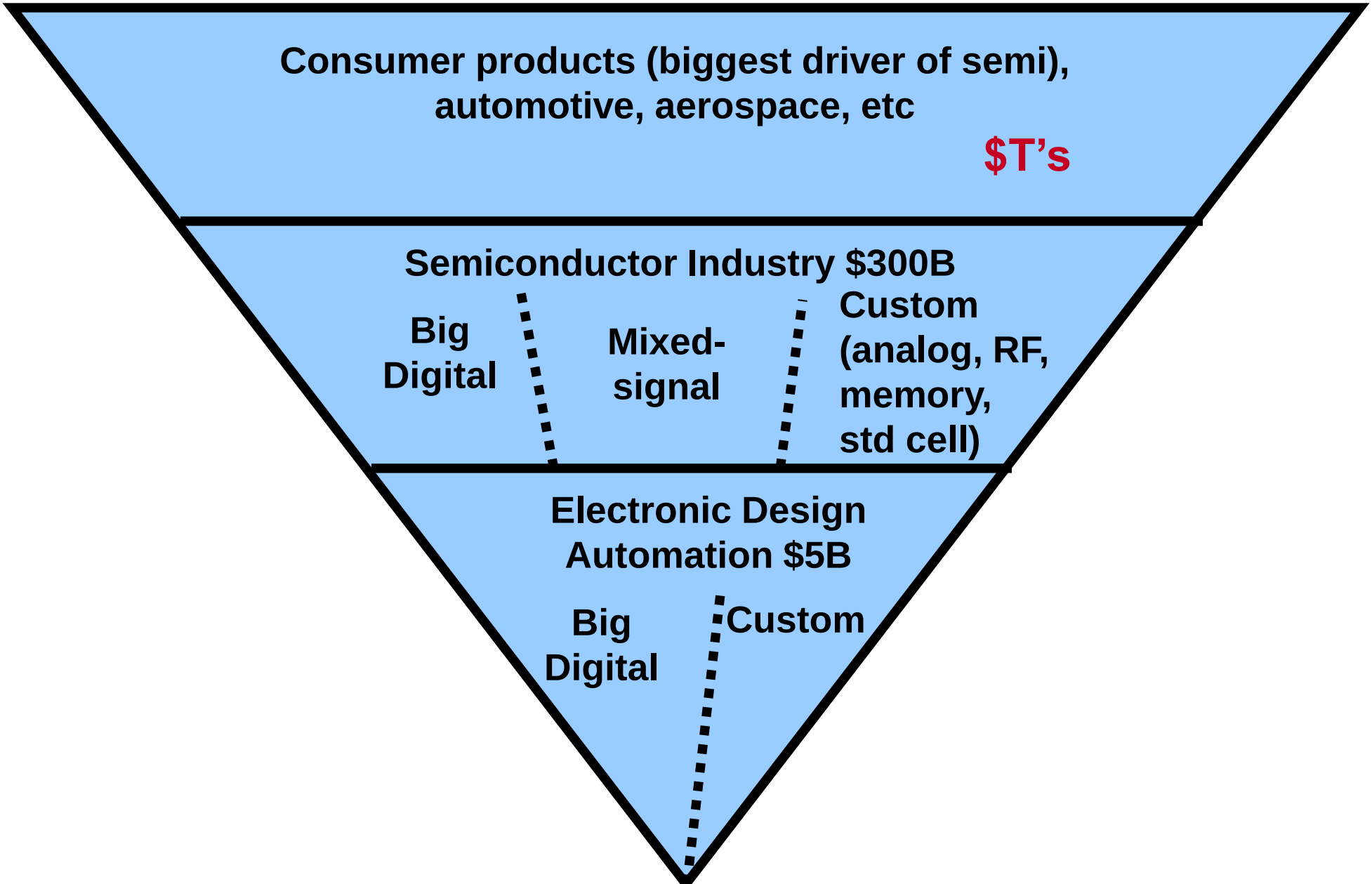


[International Technology Roadmap for Semiconductors, 2011]

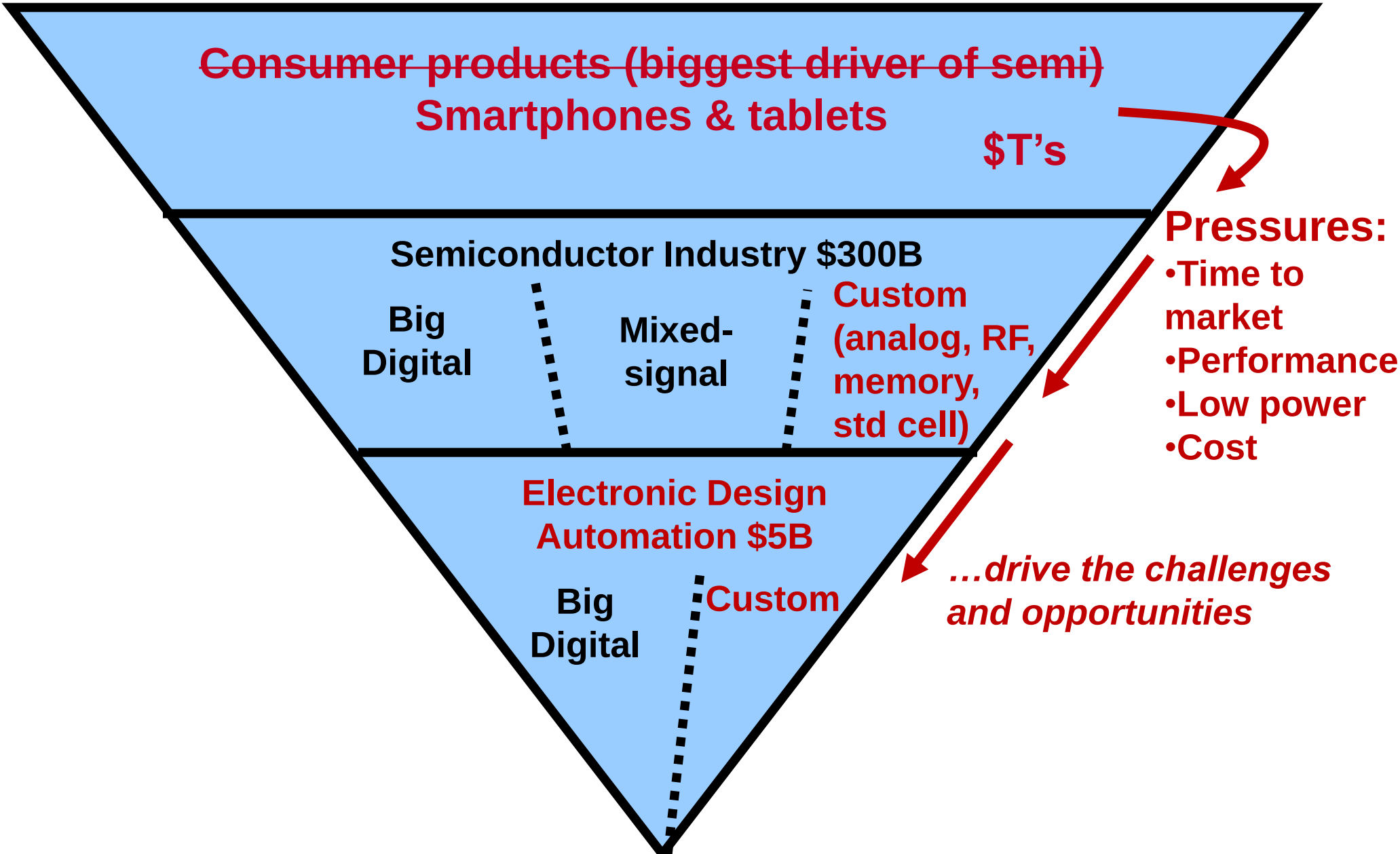

Redux:
The Moore's Law of DNA Sequencing
Cost of Sequencing One Human Genome
1E+12
1E+11
1E+10
1E+9
1E+8
1E+7
1E+6
1E+5
1E+4
1E+3
1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030 2035 2040
1.5x / year
To 10x / year
Because it touched the real Moore's Law!
[Church]

Why
Moore's Law?

Market Motivations



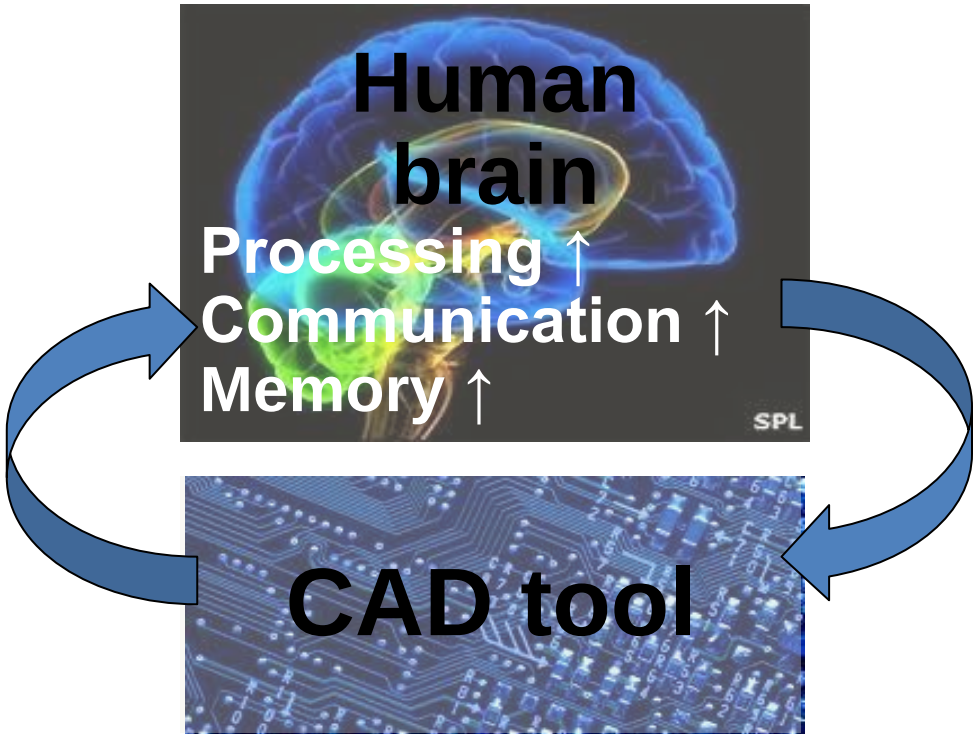
Market Motivations



Computer-aided design (CAD) tools *cognitively enhance* designers' abilities

Examples:

- **Predict the effect of manufacturing**
- **Visualize circuit behavior**



solido DESIGN AUTOMATION

Products Technology Cases About Media

Solido Solutions

- Memory
- Standard Cell
- Analog/RF
- Book

SYNOPSYS Integrated with HSPICE, FineSim, HSIM, XA
cadence Integrated with Virtuoso
berkeley design Integrated with AFS
Agilent Technologies Integrated with GoldenGate

BTW, I do CAD for a living

Solido News & Events

SemiWiki Oct 3, 2013 – High-sigma standard cell optimization
DeepChip Sept 27, 2013 – Solido ranked top 4 tool at DAC
SemiWiki Sept 20, 2013 – Process variation is a yield killer
DeepChip July 11, 2013 – DAC custom design trip report
SemiWiki Jun 9, 2013 – First FinFETs manufactured at DAC
SemiWiki May 28, 2013 – Solido on DAC Top 10 Must See List
GarySmith May 21, 2013 – Solido on DAC Must See List
SemiWiki May 18, 2013 – Winning in Monte Carlo DAC Tutorial
DeepChip May 16, 2013 – Solido CTO on Solido 6-sigma
SemiWiki May 11, 2013 – Winning in Monte Carlo
SemiWiki May 2, 2013 – Solido CEO interview
DeepChip May 2, 2013 – Solido SPICE simulation reduction
SemiWiki Apr 27, 2013 – TSMC loves Solido
DeepChip Mar 28, 2013 – User on custom design
DeepChip Feb 1, 2013 – Solido ICCAD trip report
More News & Events

Solido Case Studies

NVIDIA for memory, std cell, RF design
Huawei-HiSilicon for analog design
Qualcomm for memory design
Qualcomm for custom digital design
TSMC for memory, std cell design
TSMC for memory design
TSMC for analog/RF design
GLOBALFOUNDRIES for analog/RF design
GLOBALFOUNDRIES for memory design
STARC for analog/RF design
Analog/RF design
Memory, standard cell, analog/RF design
DAC 2013 2012 2011 2010 customer reviews
Cooley variation panel at DAC
Survey of 486 engineers on variation

DeepChip

"The most interesting tool I saw at DAC was Solido's toolset for variation analysis. The GUI and scripts can help designers do faster variation analysis."
-Anonymous User, DeepChip

See a Video Demo

Variation-Aware Custom IC Design Book

Solido Memory Design White Paper

Solido and TSMC Webinar Presentation

Cadence Virtuoso with Solido White Paper

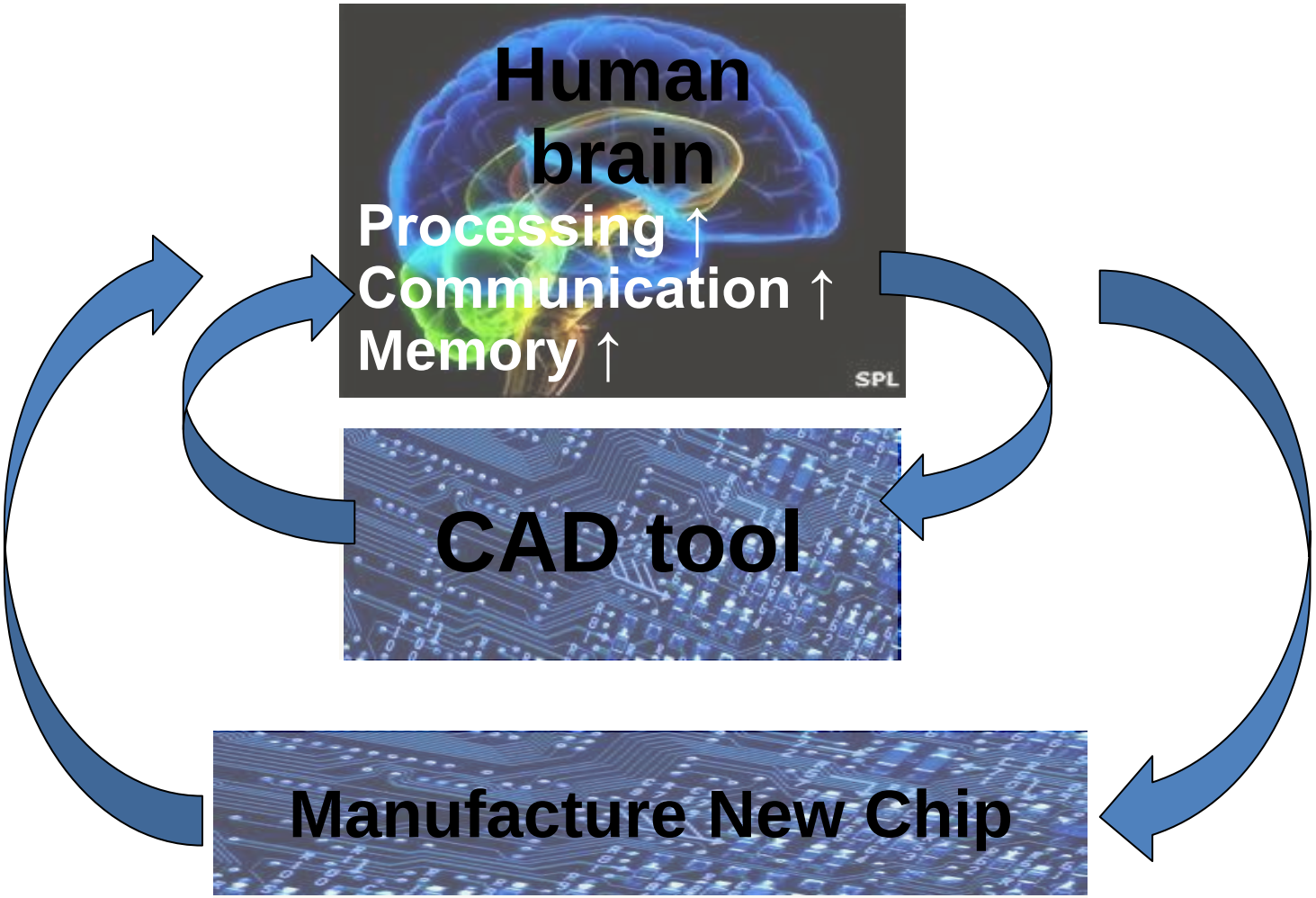
Synopsys HSPICE with Solido White Paper

in Following

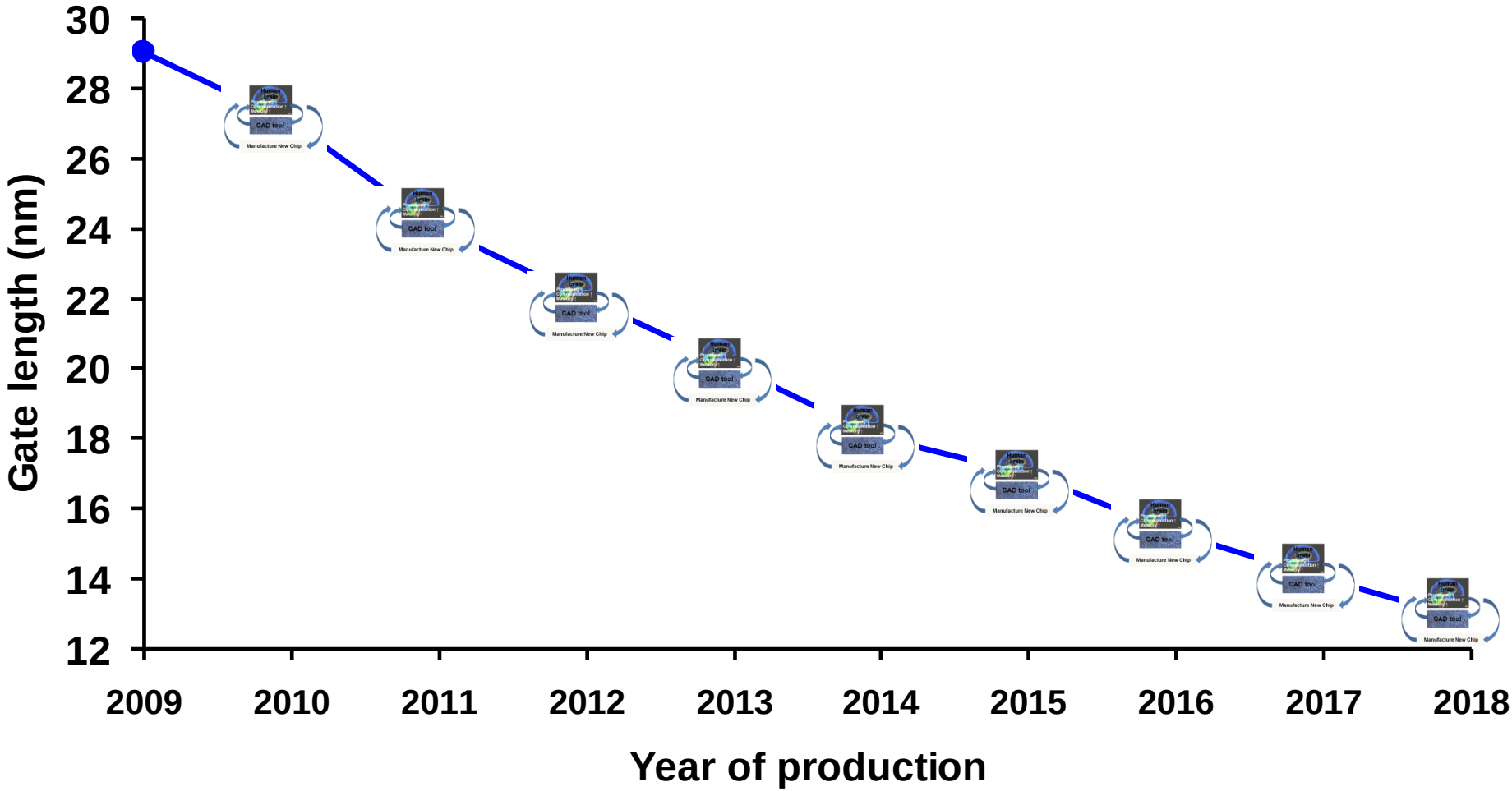
Jobs Contact Support

Computer-aided design (CAD) tools *cognitively enhance* designers' abilities

Then we build a chip.
We can use those chips to design on. It bootstraps!



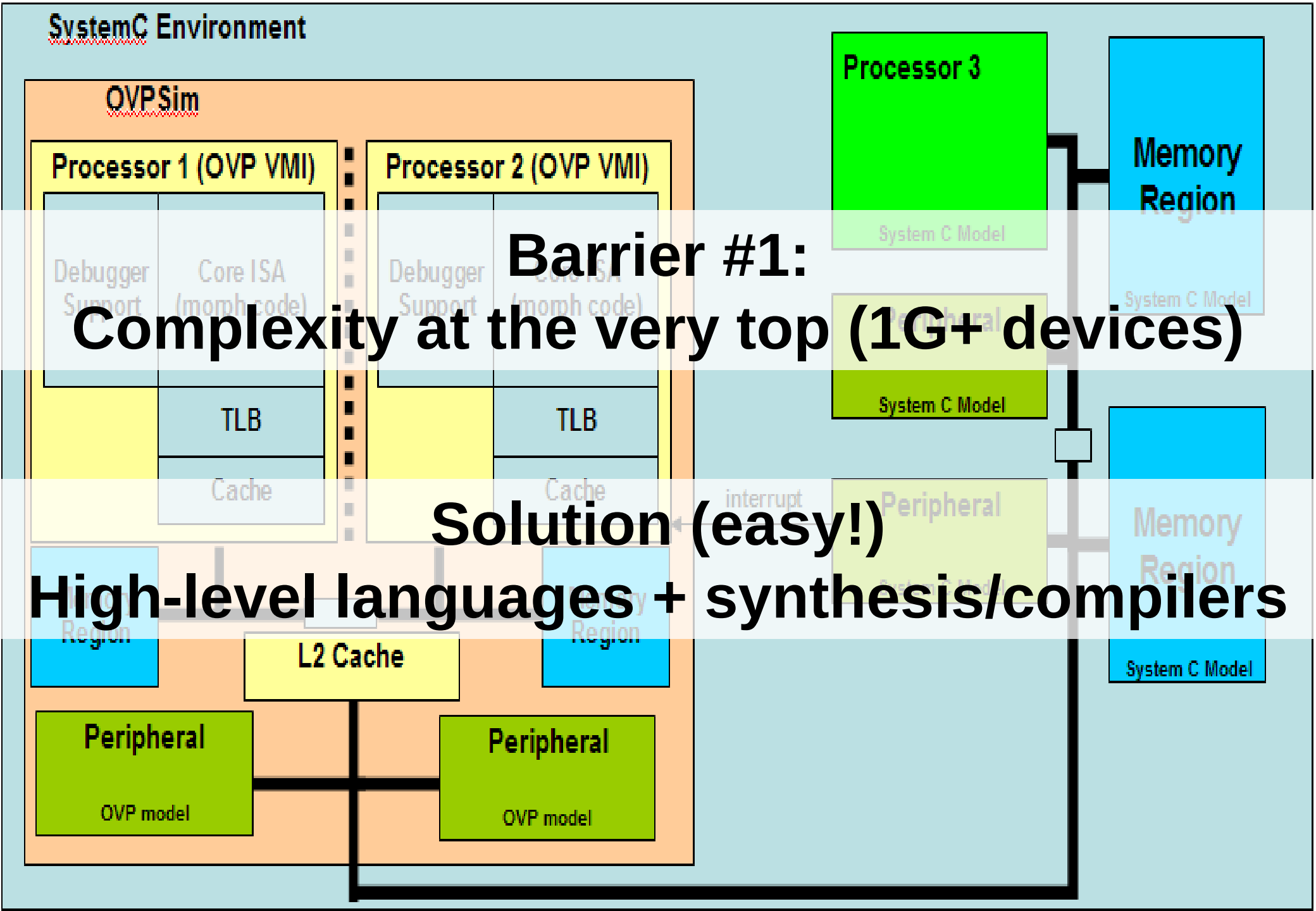
The Bootstrap



[ITRS, 2011]

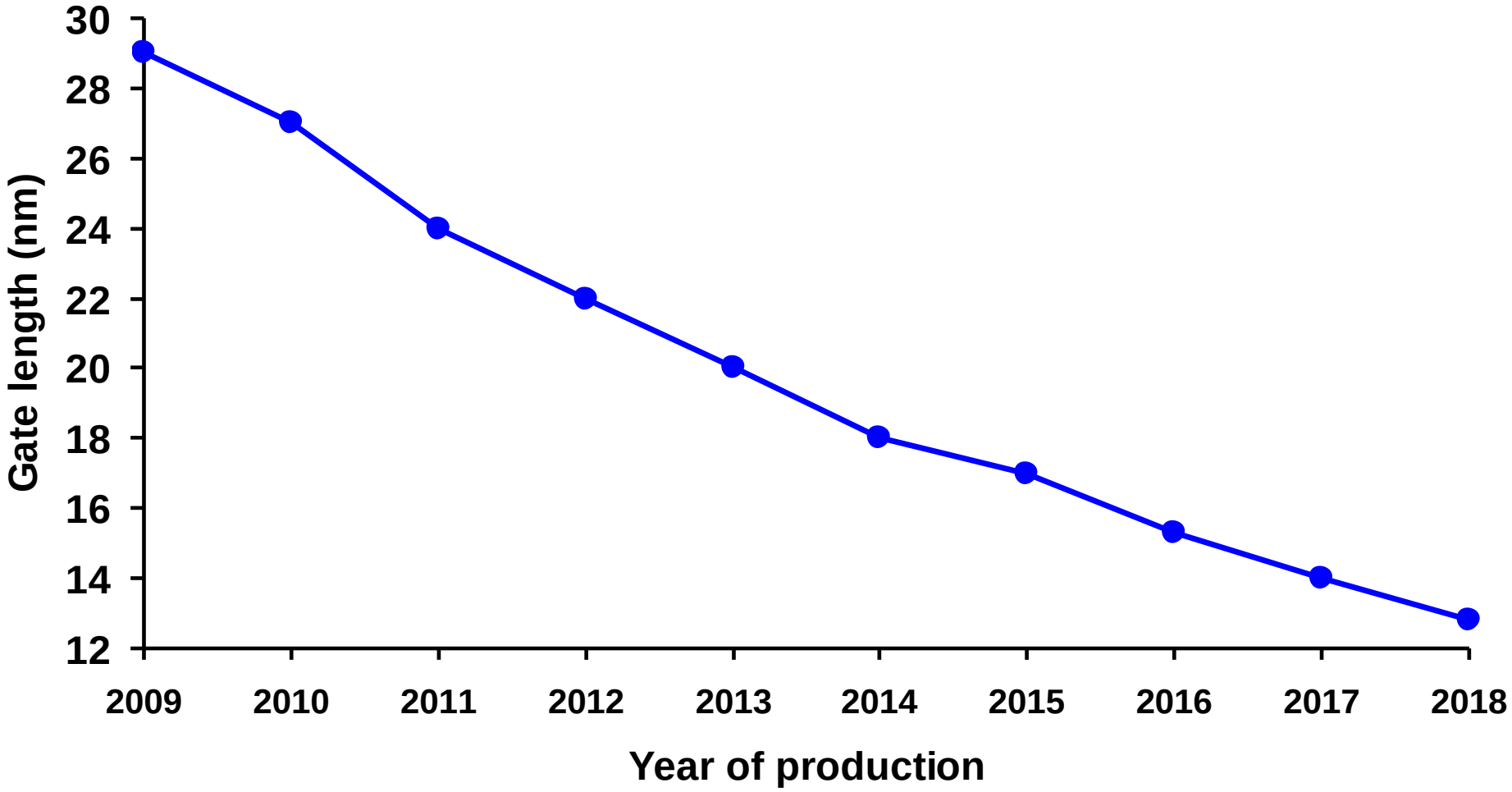
(Temporary)
Barriers to Moore's Law

Barrier #1:
Complexity at the very top (1G+ devices)


SystemC Environment
OVPSim
Processor 1 (OVP VMI)
Processor 2 (OVP VMI)
Debugger Support
Core ISA (morph code)
TLB
Cache
interrupt
L2 Cache
Peripheral
OVP model
Processor 3
System C Model
Memory Region
Barrier #1:
Complexity at the very top (1G+ devices)
Solution (easy!)
High-level languages + synthesis/compilers

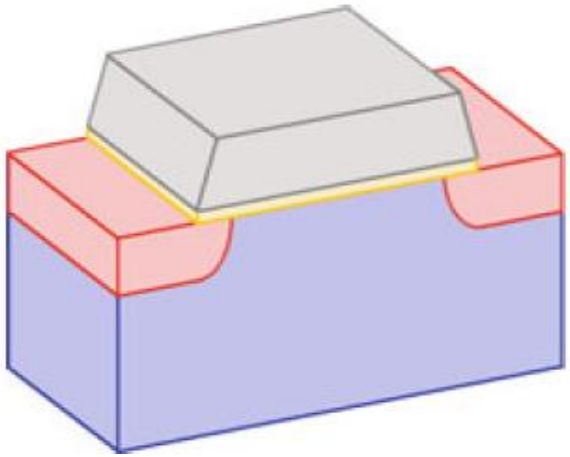
Barrier #2:
Complexity at the very bottom: variation a.k.a. physics gone mad

Transistors Are Shrinking…

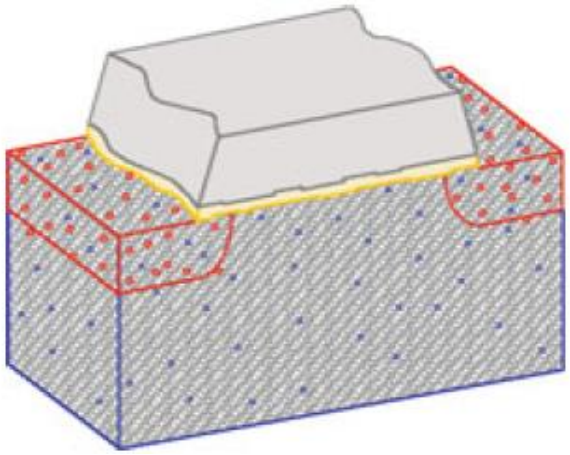


[ITRS, 2011]

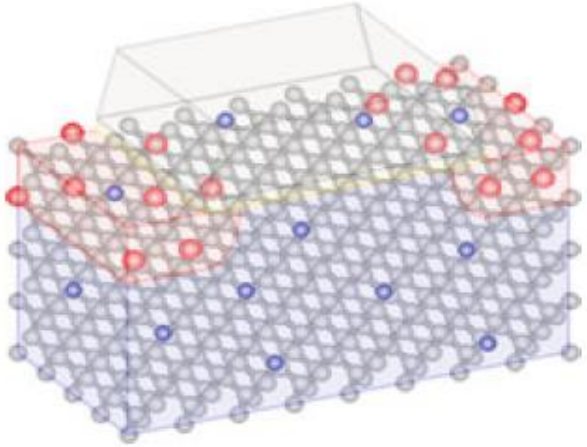
Transistors are shrinking
But atoms aren't!



traditional



22nm

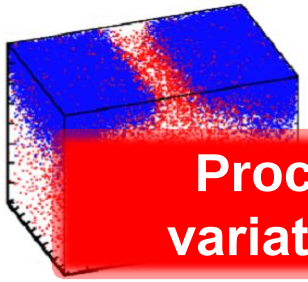


sub 10 nm (2020)

A. Asenov, "Statistical Nano CMOS Variability and Its Impact on SRAM", Chapter 3, A. Singhee and R. Rutenbar, Eds., Extreme Statistics in Nanoscale Memory Design, Springer, 2010

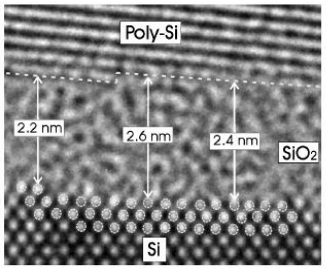
Variation = atoms out of place

…Propagating from devices to performance & yield

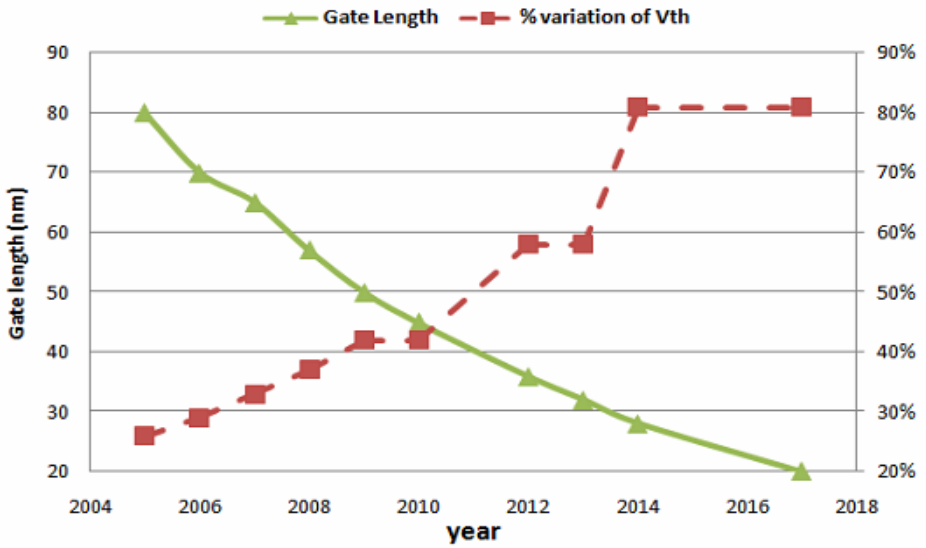


Process variation ↑

Random dopant effects

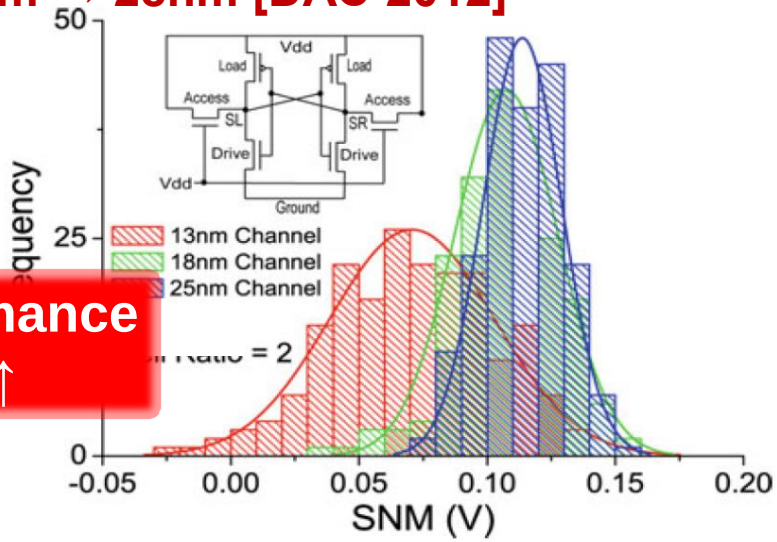


Oxide thickness



Device performance variation ↑

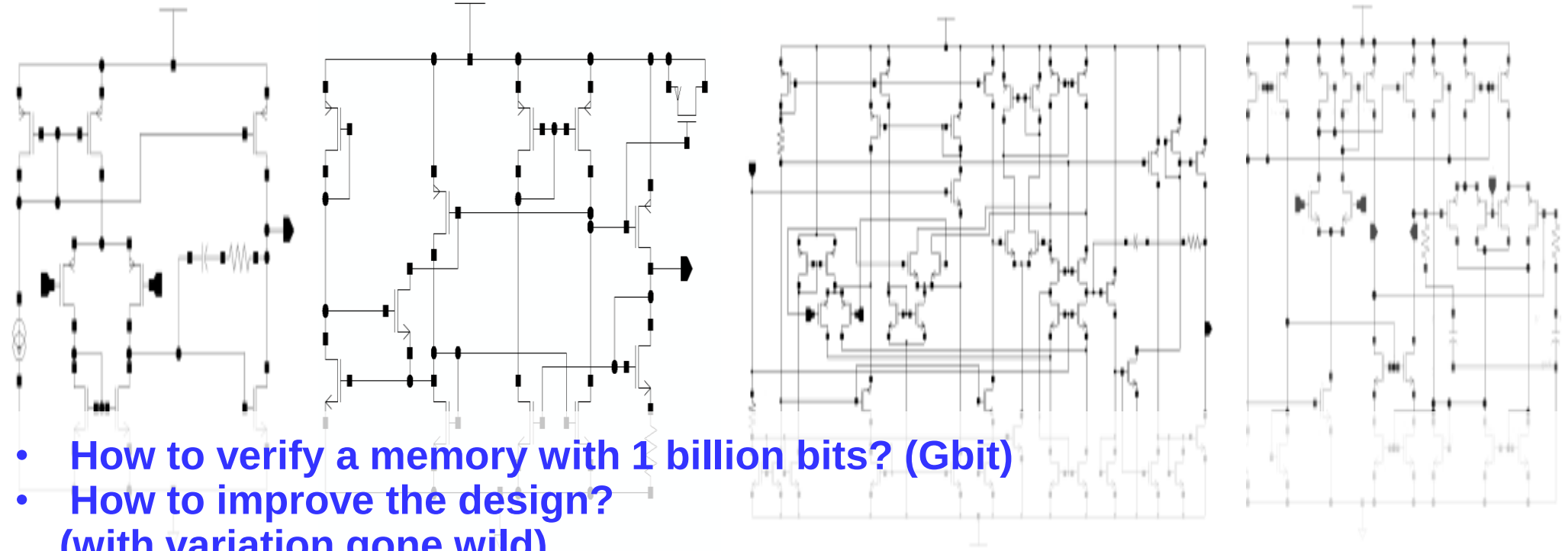
Example: GF idsat variation 2x 40nm → 28nm [DAC 2012]



Circuit performance variation ↑

-A. Asenov, "Statistical Nano CMOS Variability and Its Impact on SRAM", Ch. 3, A. Singhee and R. Rutenbar, Eds., Extreme Statistics in Nanoscale Memory Design, Springer, 2010
-C. Visweswariah, "Mathematics and Engineering: A Clash of Cultures?", IBM, 2005
-ITRS, 2006

Variability-Related Circuit Design Challenges



- How to verify a memory with 1 billion bits? (Gbit)
- How to improve the design?
  (with variation gone wild)

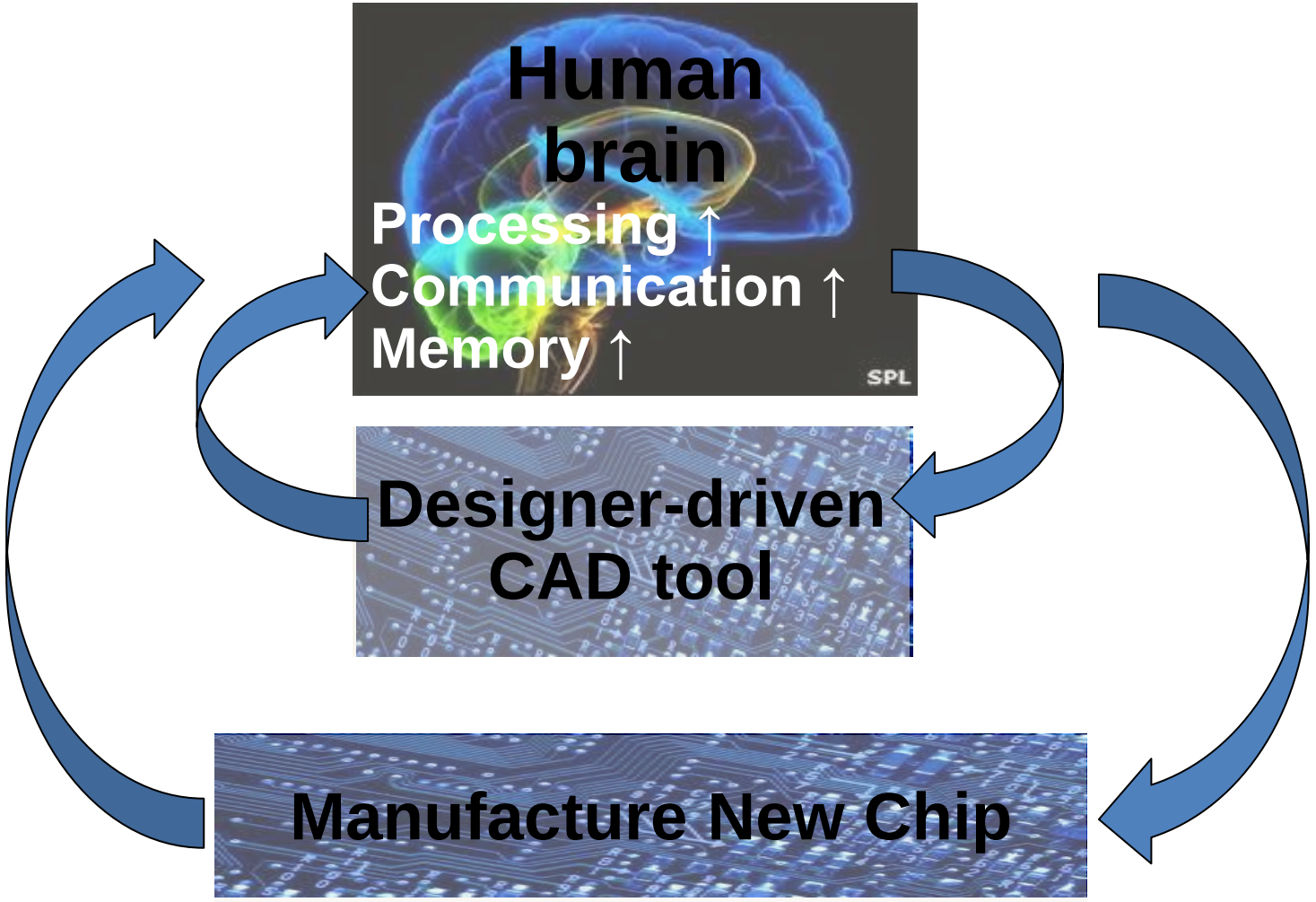
- How to verify a PLL with 3375 PVT corners?
- How to improve the design?
  (with variation gone wild)

- To get lower power, lower delay, lower area, all in less time?

Barrier #2:
Complexity at the very bottom:
variation a.k.a. physics gone mad

Solution:
Traditional CAD tools?

Q: Can (traditional) Computer-aided design (CAD) tools solve the variability problem?

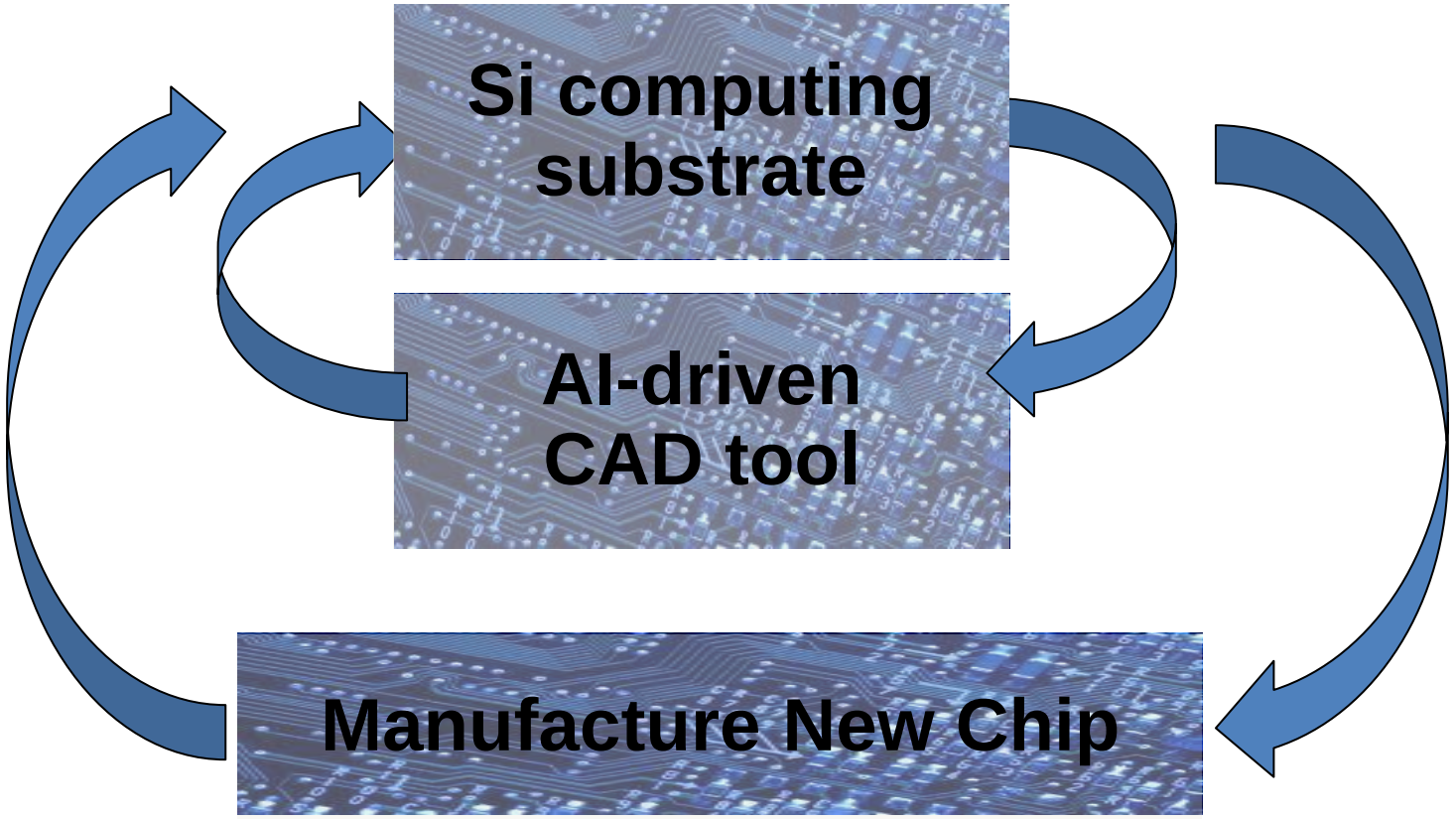


A: No. Our brains cannot process all the information needed for design. (It's been tried).

Barrier #2:
Complexity at the very bottom:
variation a.k.a. physics gone mad

Solution:
Artificial Intelligence (AI)?

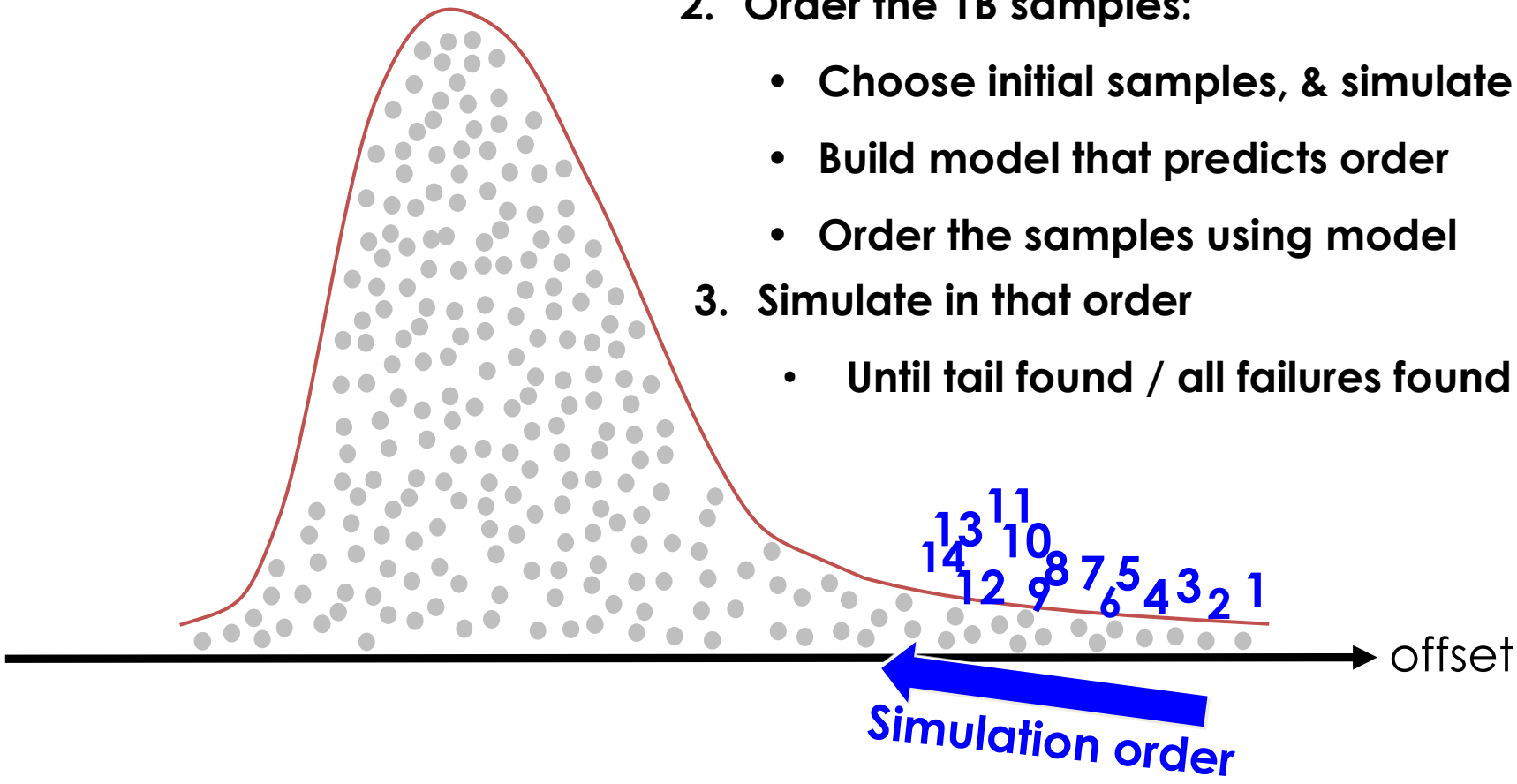
AI-driven Computer-aided design (CAD) tools



Solution: AI-driven CAD tool
AI gets faster when the Si substrate faster.
No more human bottleneck!

Example: AI-Driven Variability-Aware Memory Design

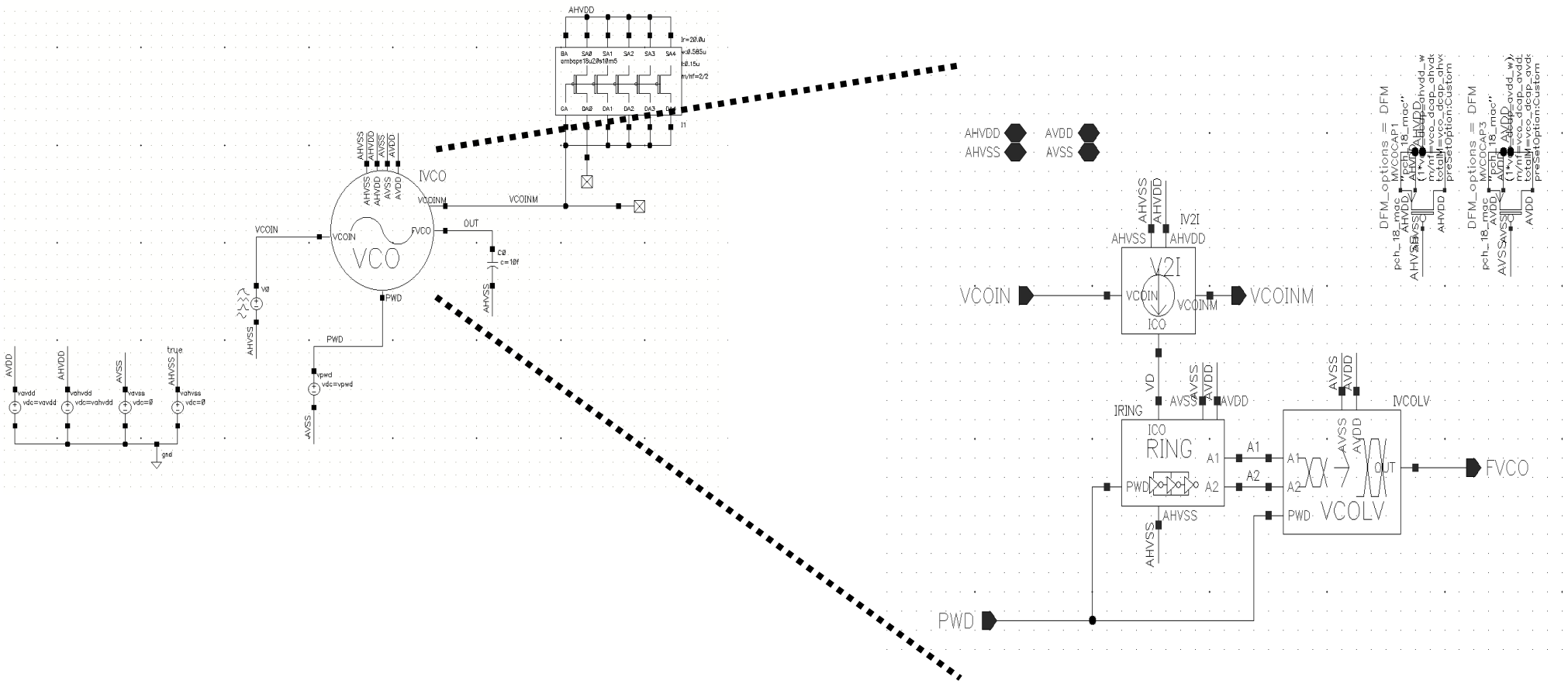
1. Generate (but don't simulate) 1B Monte Carlo samples
2. Order the 1B samples:
   - Choose initial samples, & simulate
   - Build model that predicts order
   - Order the samples using model
3. Simulate in that order
   - Until tail found / all failures found



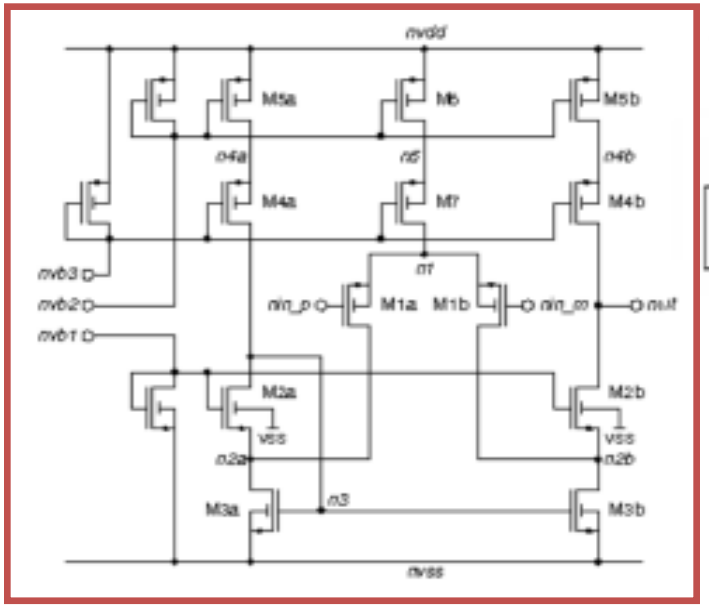
Interesting: many parallels with web search page-ranking

Example: AI-driven “corners” analysis

- TSMC 28nm, VCO of a PLL
- Specs: 48.3 < duty cycle < 51.7 %, 3 < Gain < 4.4GHz/V
- ***Traditional: 3375* PVT corners to simulate** (temp, $V_{ah,vdd}$, $V_{a,vdd}$, $V_{d,vdd,}$, and 15 model sets)
- **With AI: 275 corners to simulate, as thorough as before**



Example: AI-based whitebox models of circuits

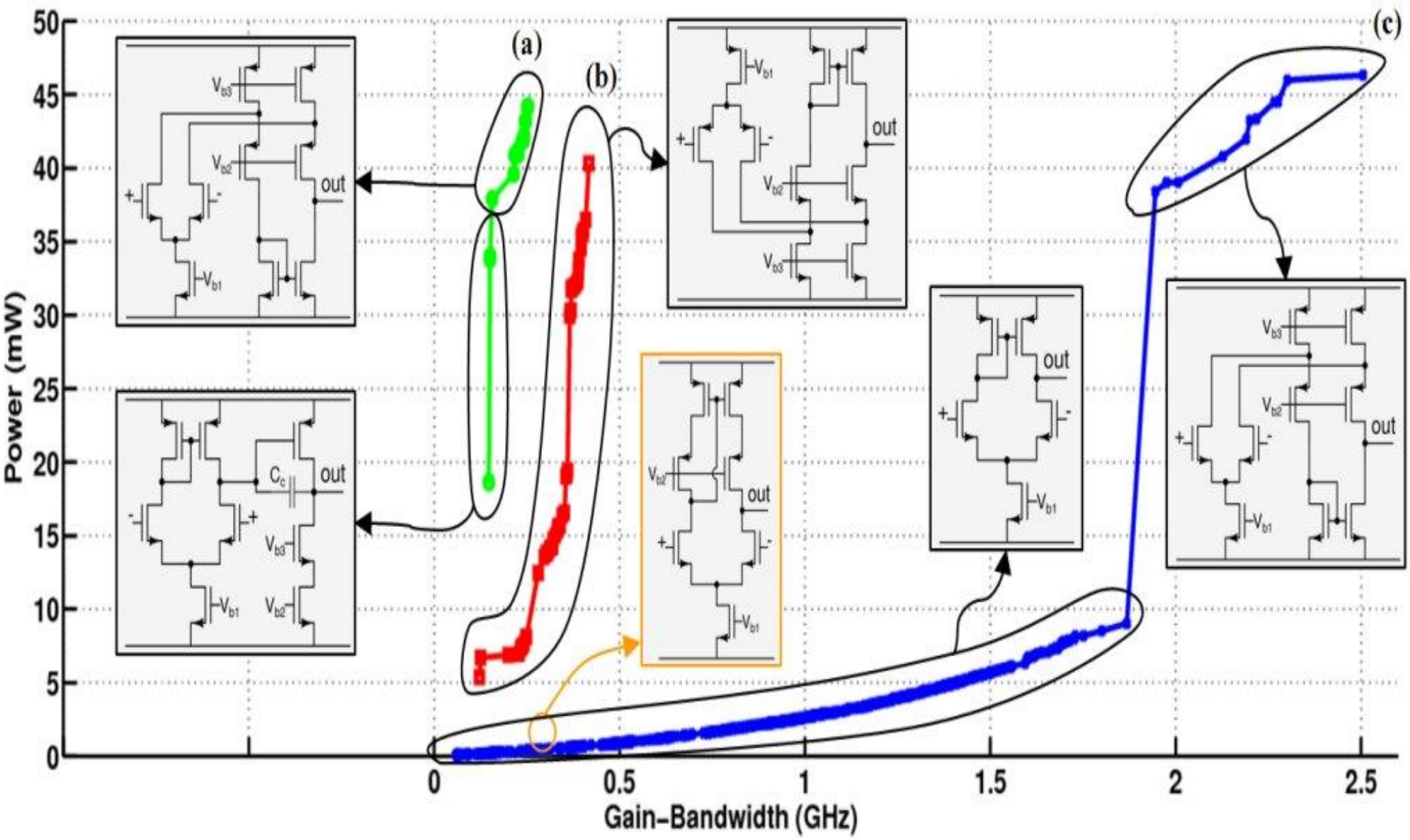


SPICE

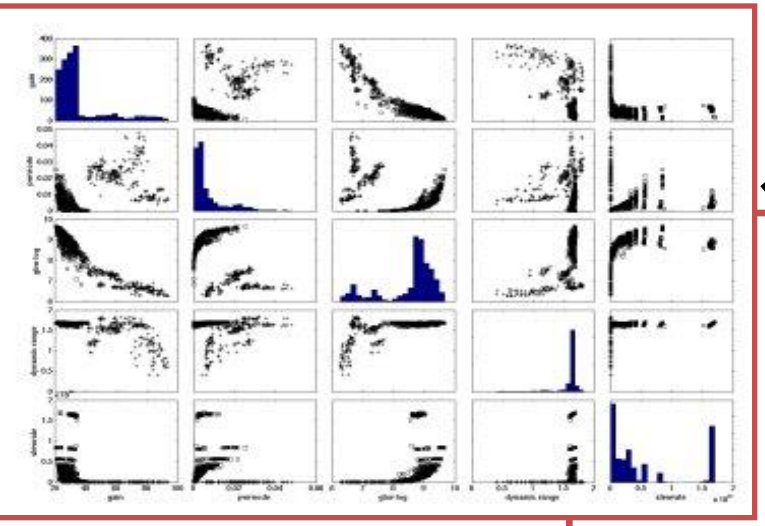
Symbolic Modeling

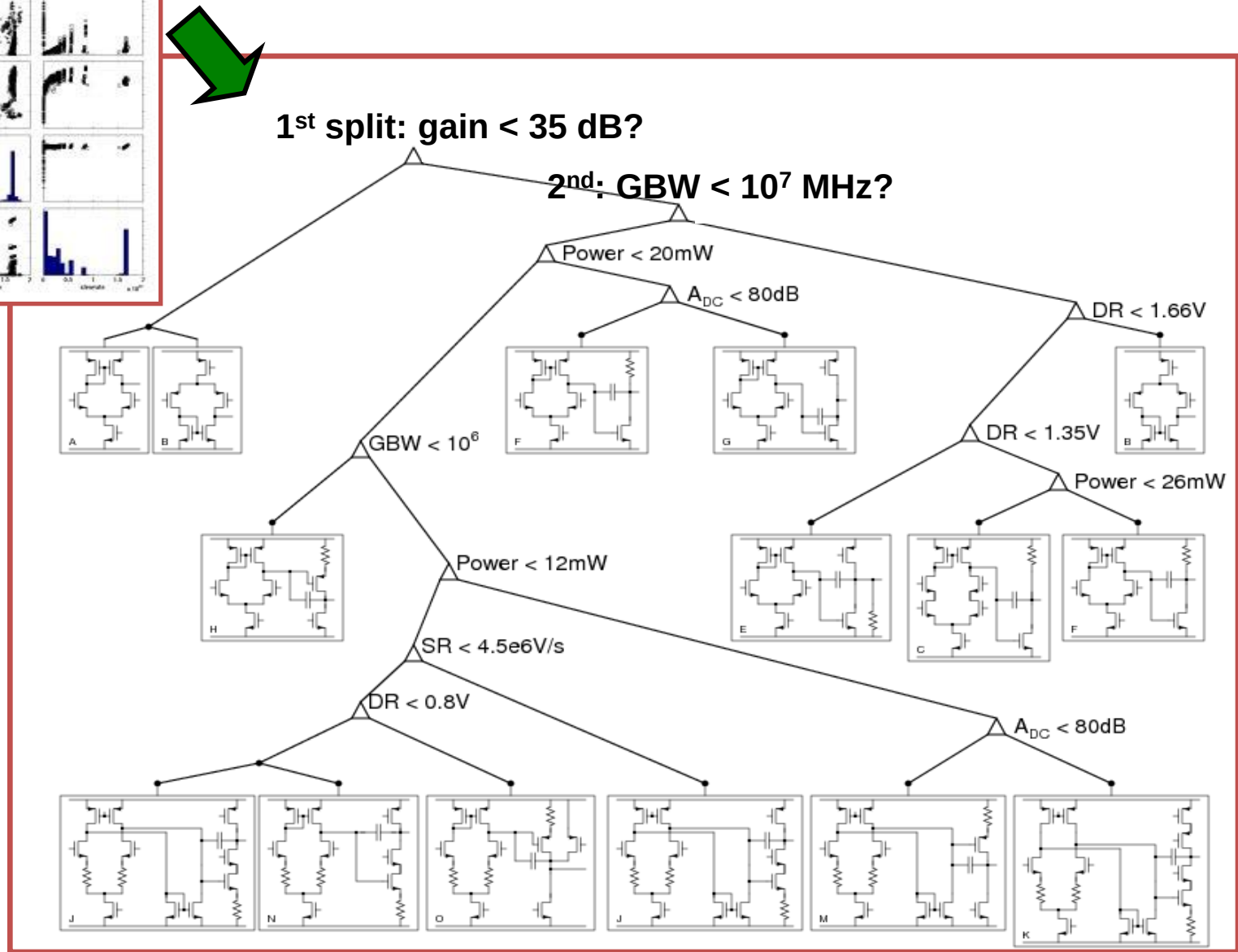
Perf.	Expression
A_{LF}	-10.3 + 7.08e-5 / id1 + 1.87 * ln(-1.95e+9 + 1.00e+10 / (vsg1*vsg3)+ 1.42e+9 *(vds2*vsd5) / (vsg1*vgs2*vsg5*id2))
f_u	10^(5.68 - 0.03 * vsg1 / vds2 - 55.43 * id1+ 5.63e-6 / id1)
PM	90.5 + 190.6 * id1 / vsg1 + 22.2 * id2 / vds2
V_{offset}	- 2.00e-3
SR_p	2.36e+7 + 1.95e+4 * id2 / id1 - 104.69 / id2 + 2.15e+9 * id2 + 4.63e+8 * id1
SR_n	- 5.72e+7 - 2.50e+11 * (id1*id2) / vgs2 + 5.53e+6 * vds2 / vgs2 + 109.72 / id1

Example: AI to synthesize analog circuit topologies



Example: AI to generate decision trees





Some AI tools that I use for circuit design
(and where else they're used)

- **Classification – Layout analysis, high-sigma analysis, Fraud detection, spam filtering …**
- **Regression – Circuit optimization, fast design sweep, high-sigma analysis, Stock prediction, sensitivity analysis …**
- **Whitebox regression – Behavioral modeling / system level simulation, Scientific discovery …**
- **Optimization – Worst-case PVT analysis, circuit cell optimization, airfoil design, circuit simulation …**
- **Structural synthesis – Analog topology synthesis, robotics …**
- **System identification – Behavioral modeling, Scientific discovery …**
- **Ranking – High-sigma analysis, Web search, ad serving, social discovery …**
- **Control – Behavioral modeling, Auto-driving autos, spacecraft trajectories …**
- **…**

The Bootstrap, on AI steroids

Each of these steps is clocked by how fast we can go through the cycle.

We are approaching an era where that clock is only the CPU clock.

(No more human bottleneck.)