Faith, Trust and Pixie Dust: Trust in Analog Computer-Aided Design

Trent McConaghy
Co-founder & CTO
Solido Design Automation

solido DESIGN AUTOMATION

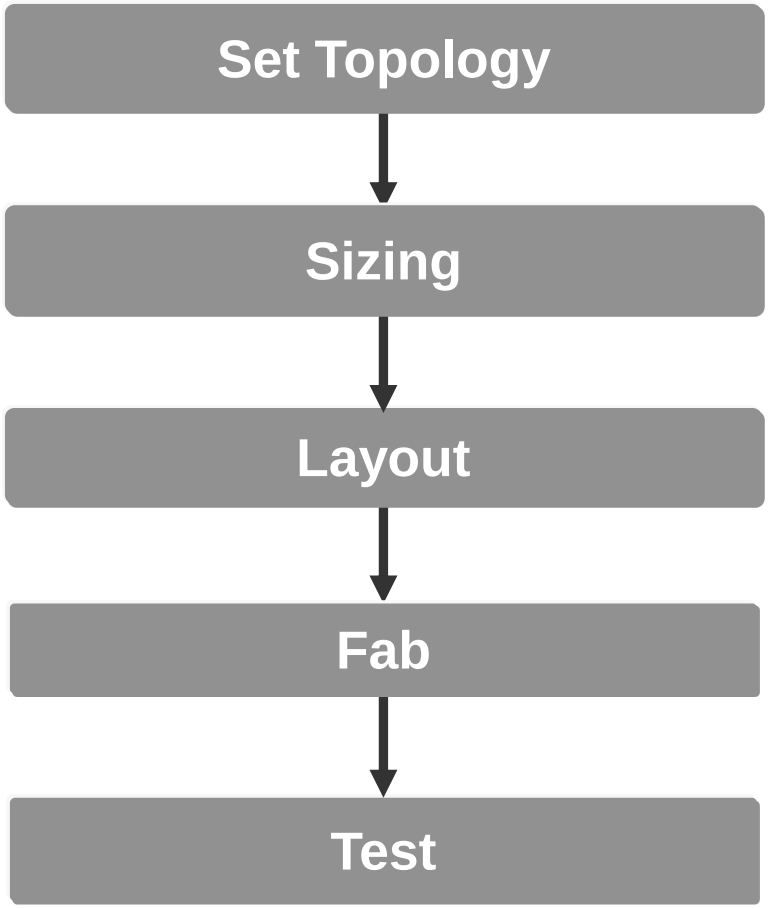
“Wanna go for a drive?”


A problem has been detected and windows has been shut down to prevent damage
to your computer.
The problem seems to be caused by the following file: SPCMDCON.SYS
PAGE_FAULT_IN_NONPAGED_AREA
If this is the first time you've seen this Stop error screen,
restart your computer. If this screen appears again, follow
these steps:
Check to make sure any new hardware or software is properly installed.
If this is a new installation, ask your hardware or software manufacturer
for any windows updates you might need.
If problems continue, disable or remove any newly installed hardware
or software. Disable BIOS memory options such as caching or shadowing.
If you need to use Safe Mode to remove or disable components, restart
your computer, press F8 to select Advanced Startup Options, and then
select Safe Mode.
Technical information:
*** STOP: 0x00000050 (0xFD3094C2,0x00000001,0xFBFE7617,0x00000000)
*** SPCMDCON.SYS - Address FBFE7617 base at FBFE5000, DateStamp 3d6dd67c
BSOD = D

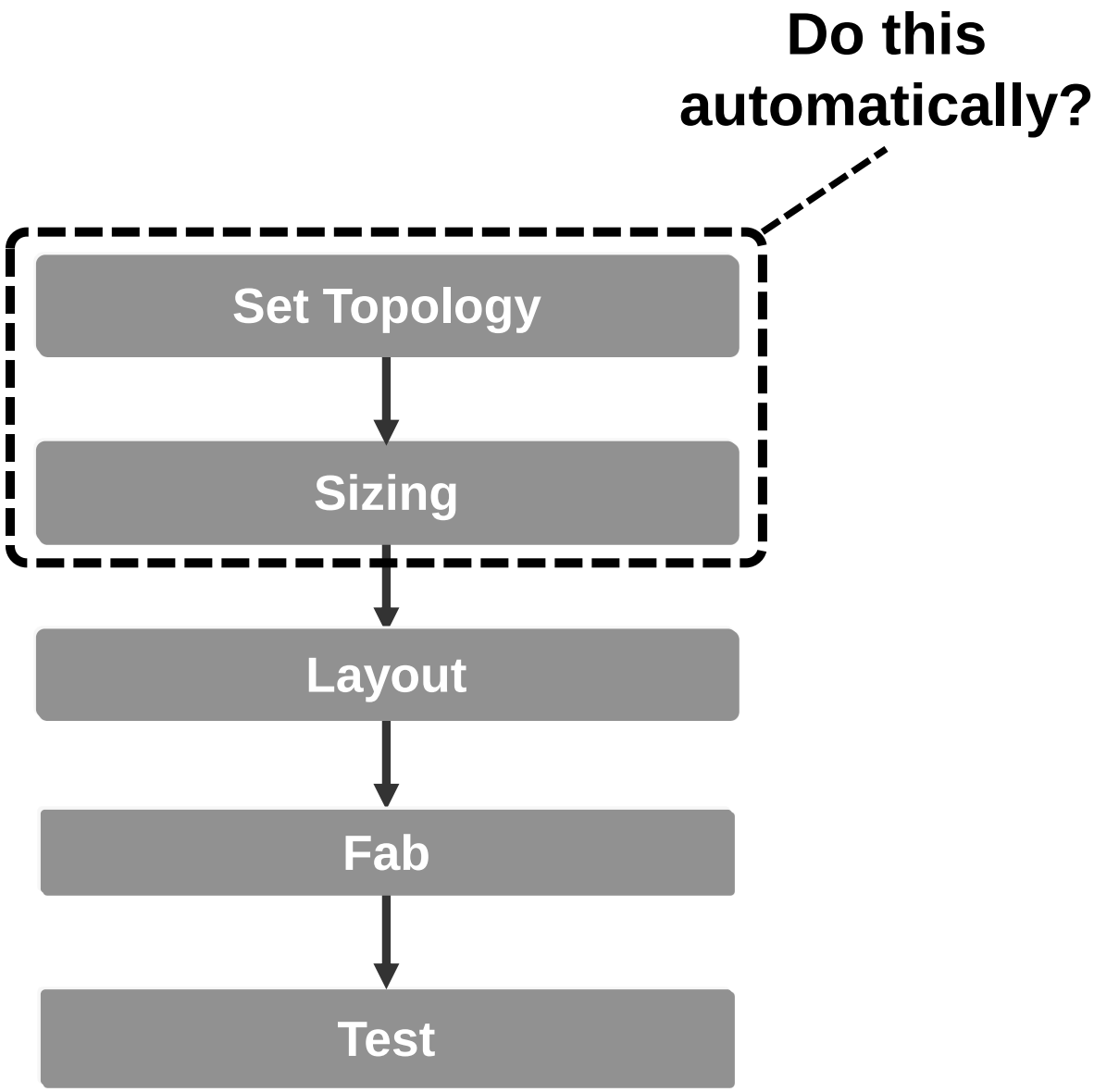
Outline: A Personal Story

- **Analog Topology Synthesis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**
- **High-Sigma Analysis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**

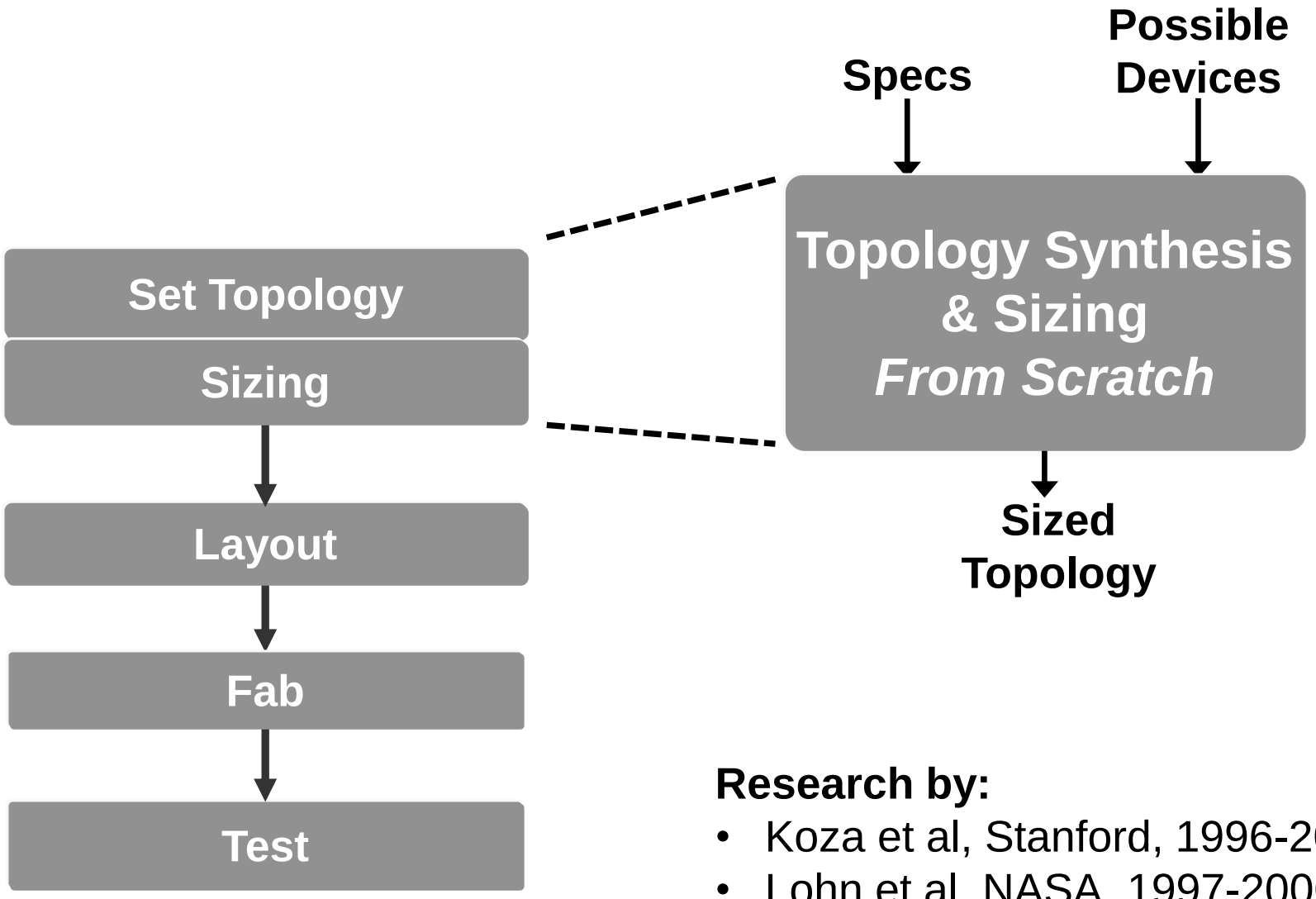
Traditional Analog Flow



The Dream



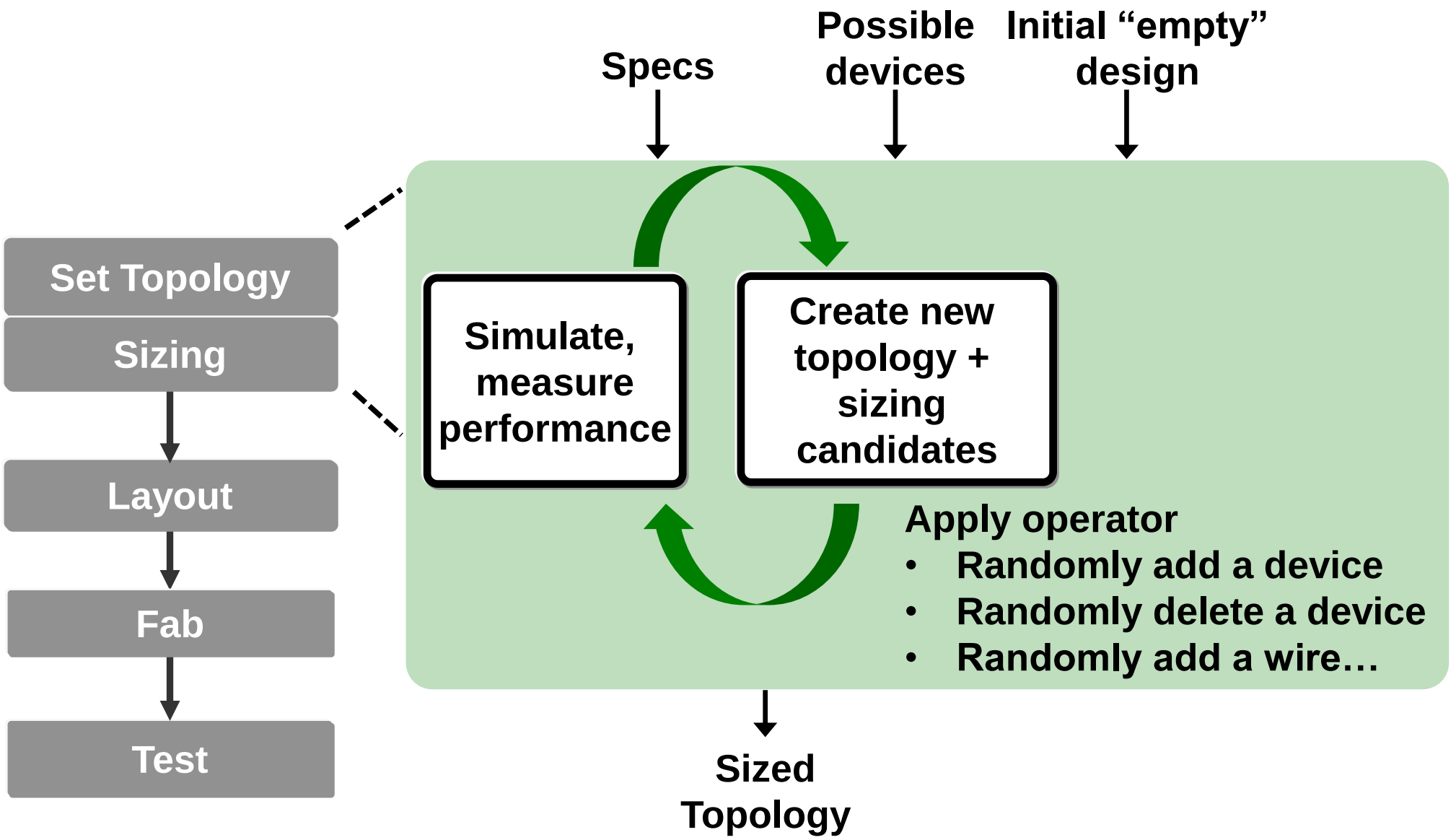
The First Cut: Frame as "Open-Ended" Problem



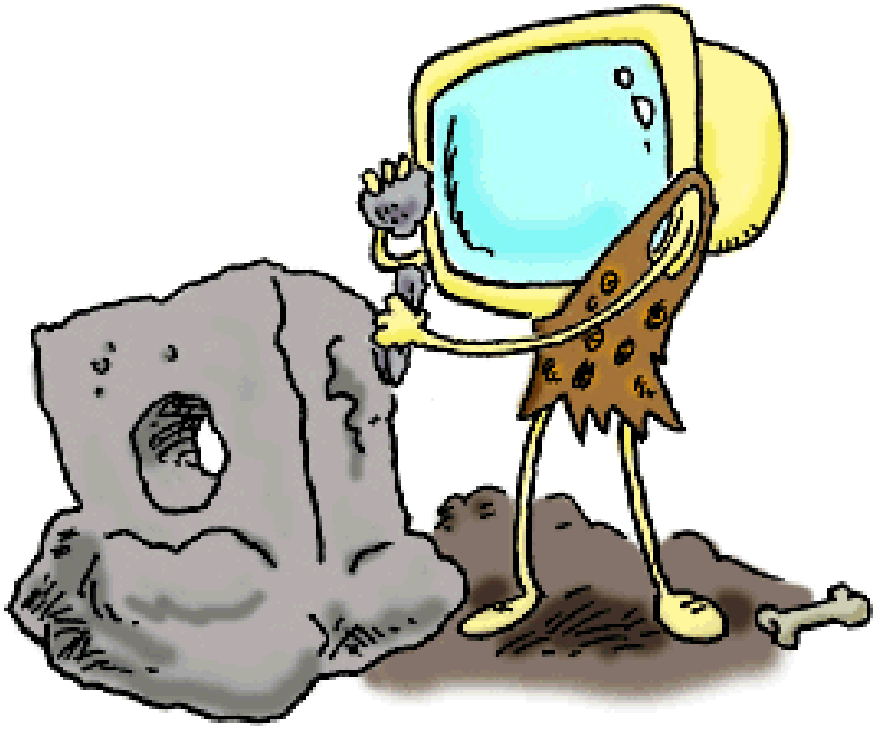
Research by:

- Koza et al, Stanford, 1996-2006
- Lohn et al, NASA, 1997-2000
- **Myself & colleagues, ADA, 1998-1999**
- ≈a dozen other labs up to present

The First Cut: Solving "Open Ended" Problem

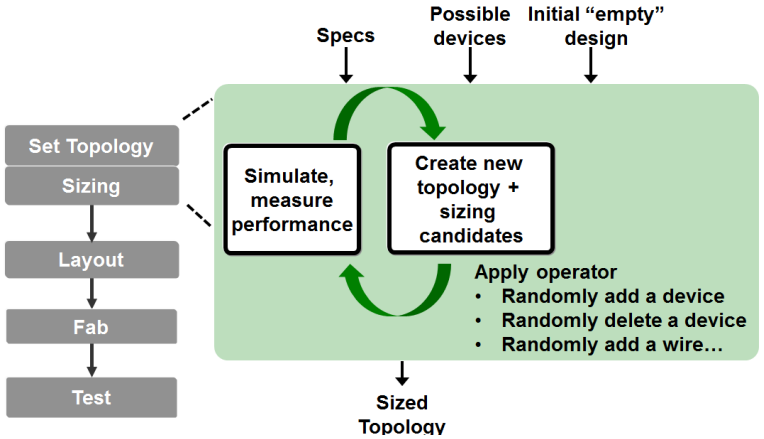


Reinvention takes computational effort



Takes a lot more computational effort to “try to get a guarantee” (though still no guarantee)

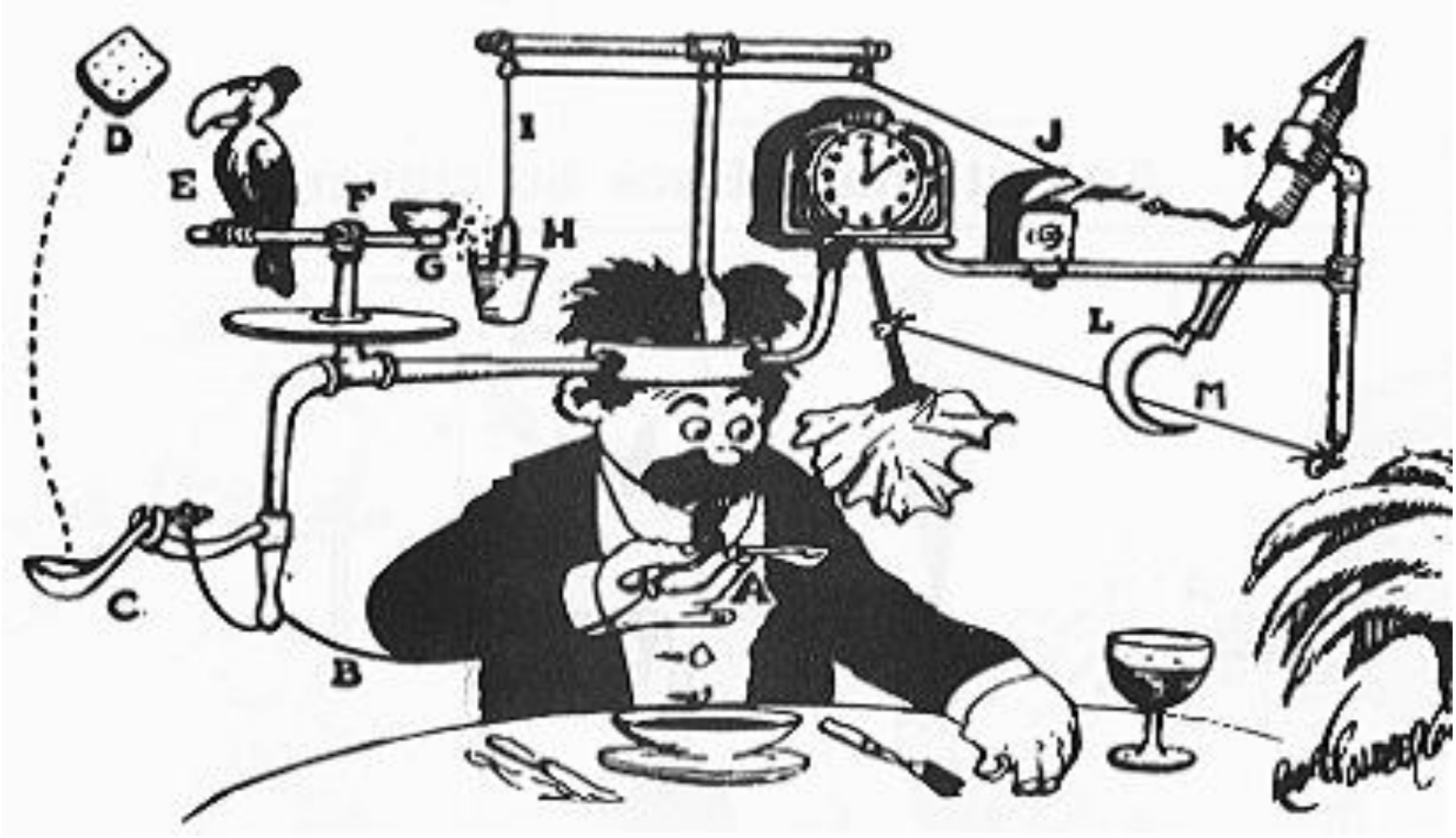
Research Focus: Speed



- **Koza et al, Stanford, 1996-2006**
  Runtime 1 week on 1000 cores
- Lohn et al, NASA, 1997-2000
- **Myself & colleagues, ADA, 1998-1999**
  Runtime 15 min on 30 cores
- ≈a dozen other labs up to present
  Speed, speed, speed

Reinvention isn’t guaranteed

Trustworthy designs are the problem!!!



Dangling resistors, G to G, … illogical, complex

How to get trustworthy designs?

Add constraints

Run again

How to get trustworthy designs?

Add constraints

Run again, see more problems

Add constraints

Run again

My experience #1

Add constraints

Run again, see more problems

Add constraints

Run again, see more problems

Add constraints

Run again, more problems

Add constraints

(Think whack-a-mole)

My experience #2

ADA: Wanna buy our synthesis tool?

Customer: how can I trust it?

ADA: Uhhh… you gotta have faith?

Customer: <click>

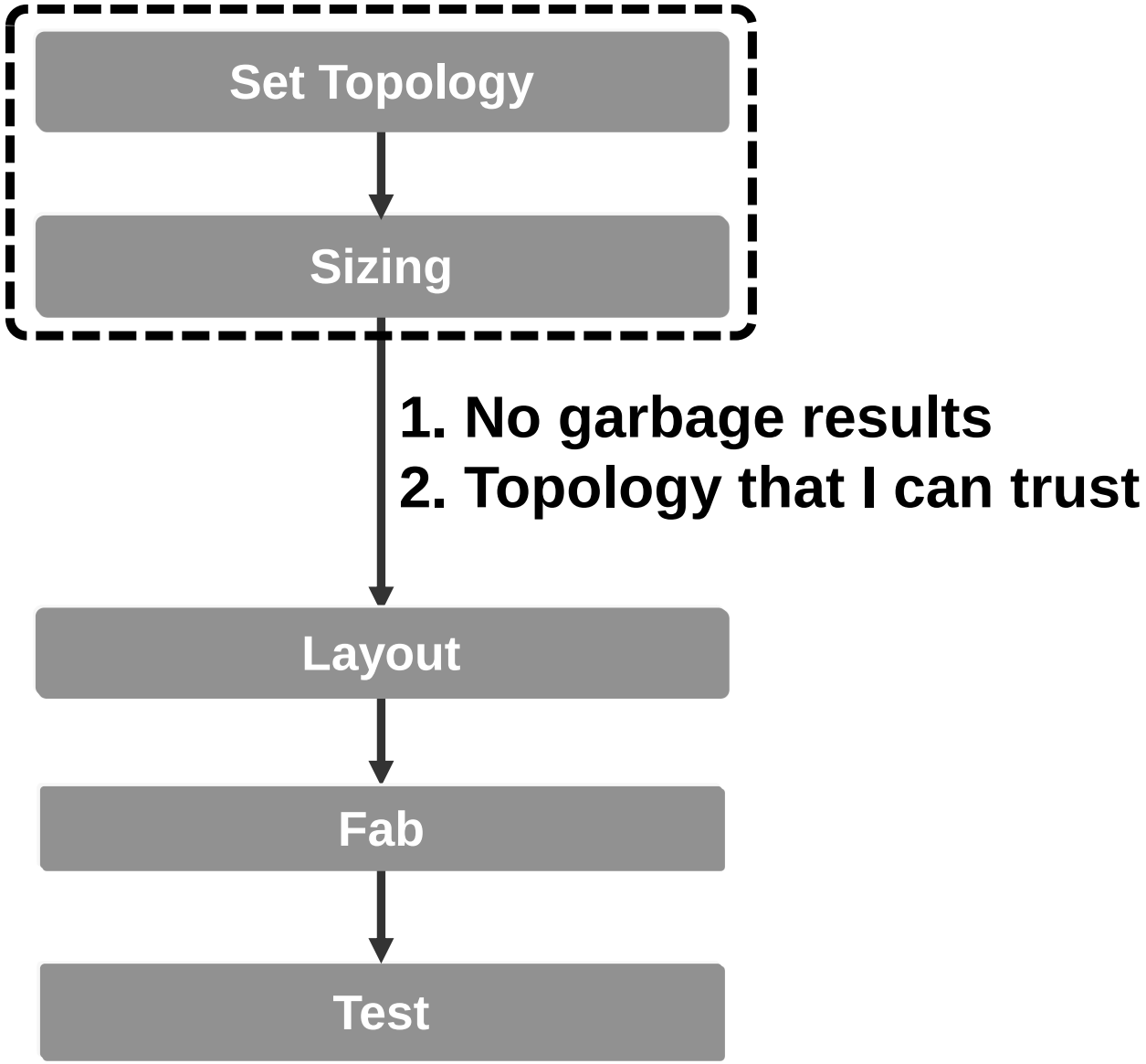
The futility…

ADA: <stops topology synthesis project>

Outline: A Personal Story

- **Analog Topology Synthesis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**
- **High-Sigma Analysis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**

Rethinking Topology Synthesis Problem



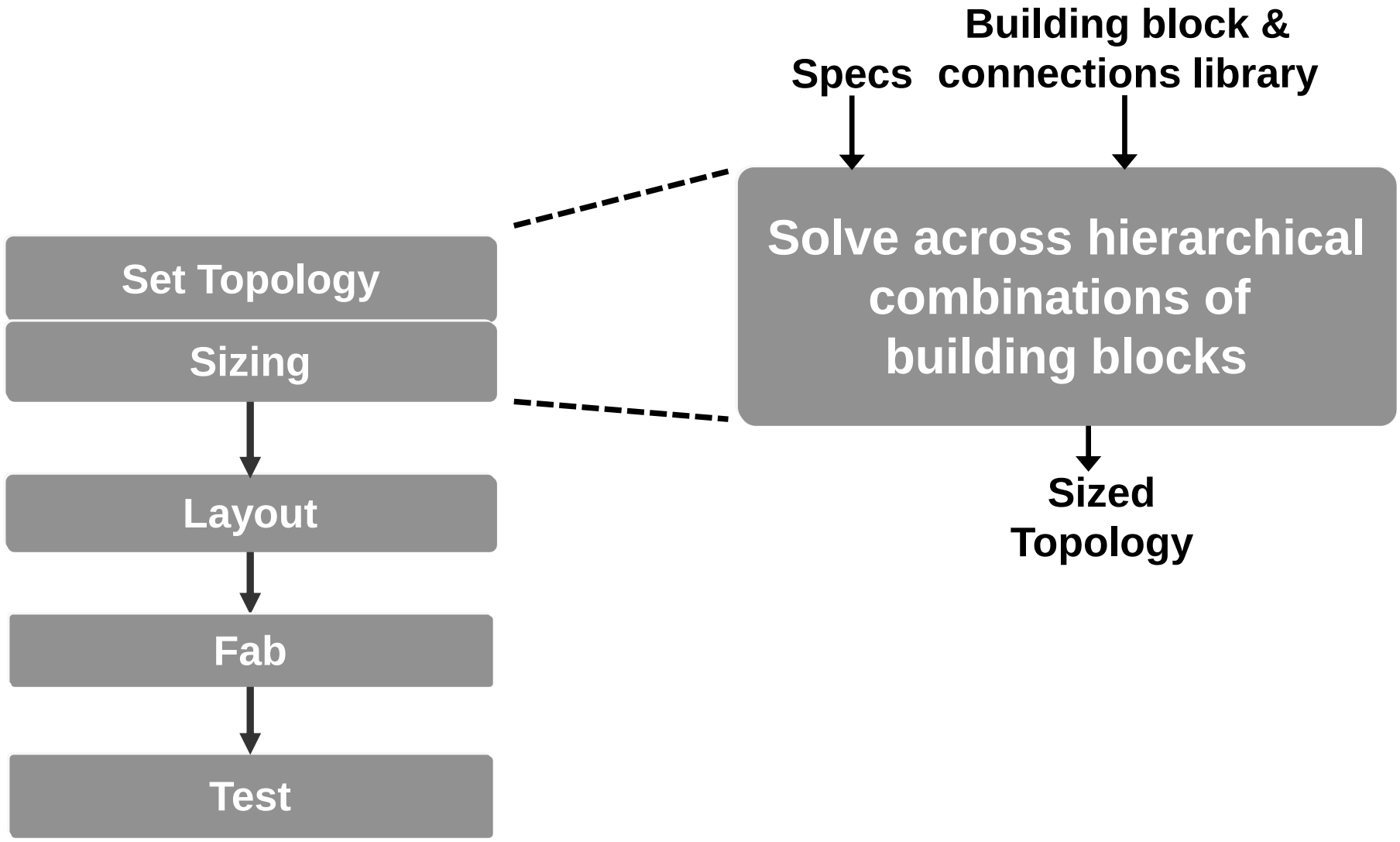
Rethinking Topology Synthesis: Approach

- **Q: When a designer "selects" a topology, where does he get it from?**
- **A: It's a combination of building blocks, connected not-insanely.**

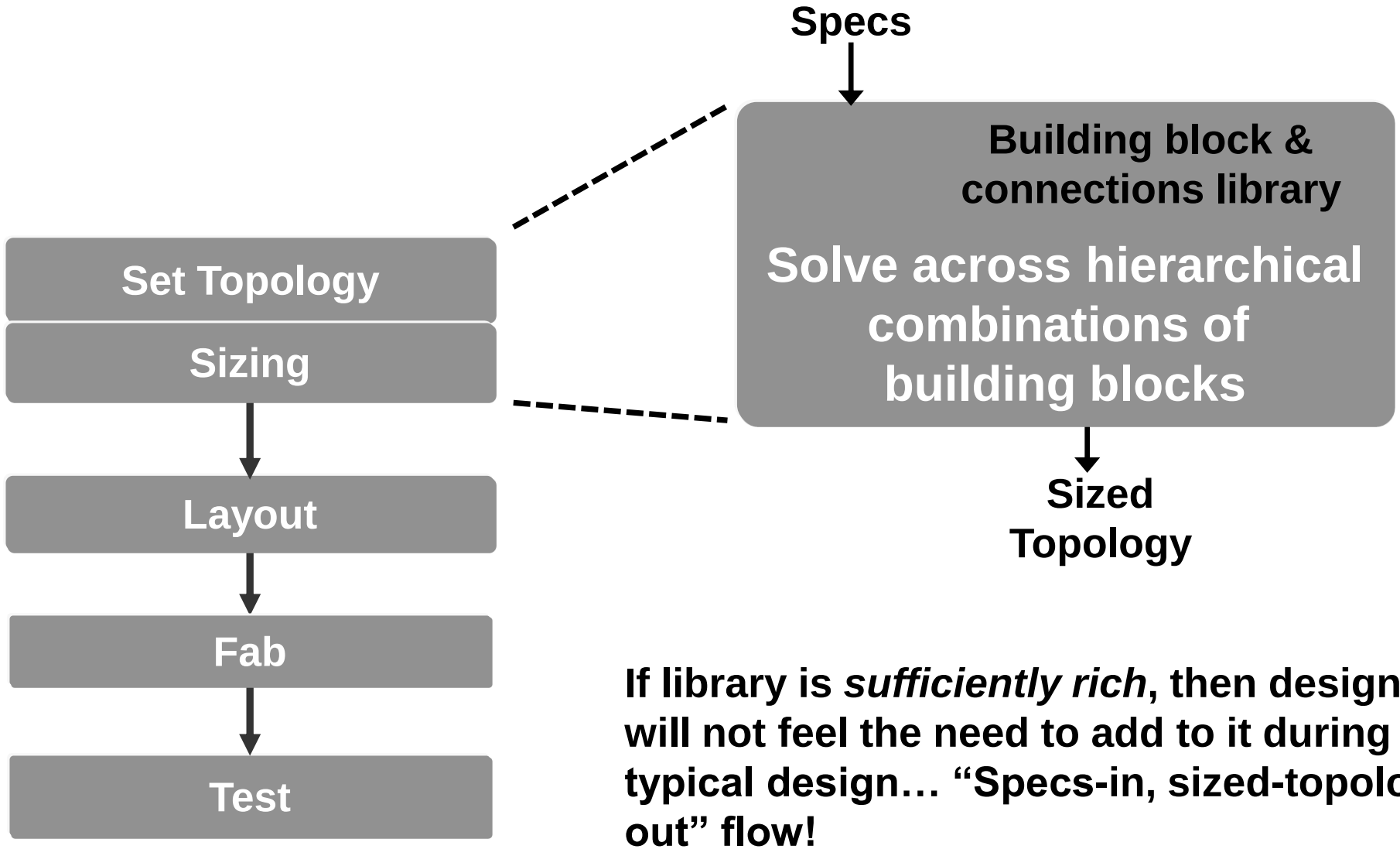
  Current mirrors, diff pairs, cascoding, feedback, etc.
- **That is,**
  - **Trustworthy building blocks**
  - **With trustworthy connections**
  - **(Organized hierarchically)**

Let's constrain synthesis space to that!

Rethinking Topology Synthesis: Approach



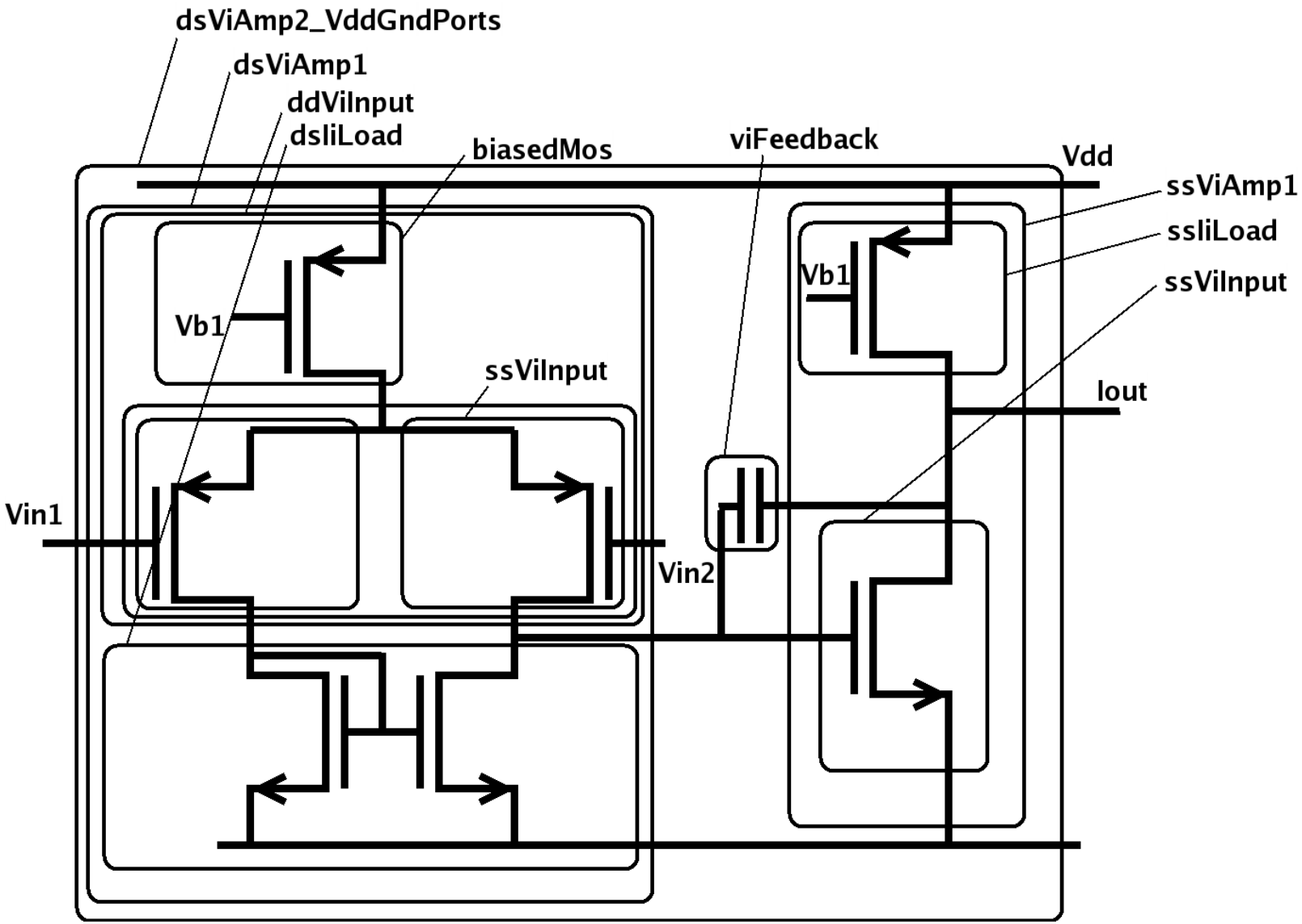
Rethinking Topology Synthesis: Approach



If library is *sufficiently rich*, then designers will not feel the need to add to it during typical design… "Specs-in, sized-topology out" flow!

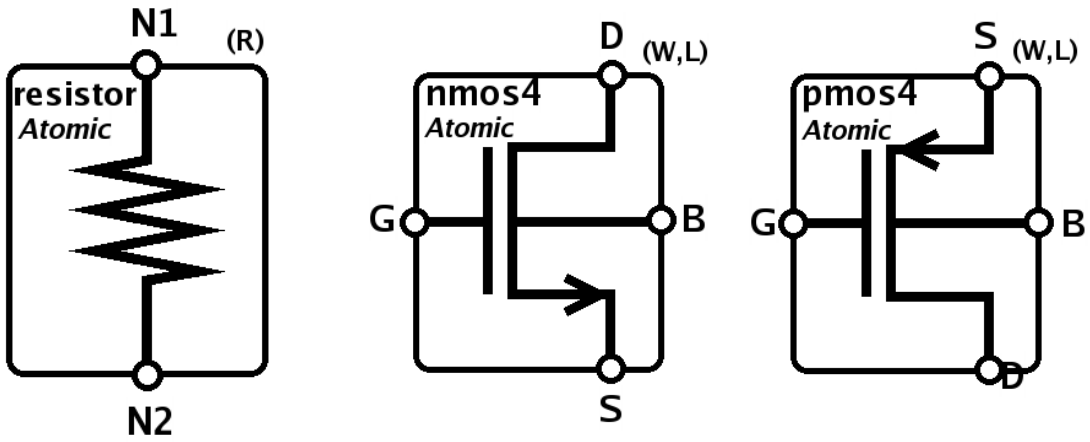
Can we make the library sufficiently rich?

Example breakdown of a “Miller Op Amp”

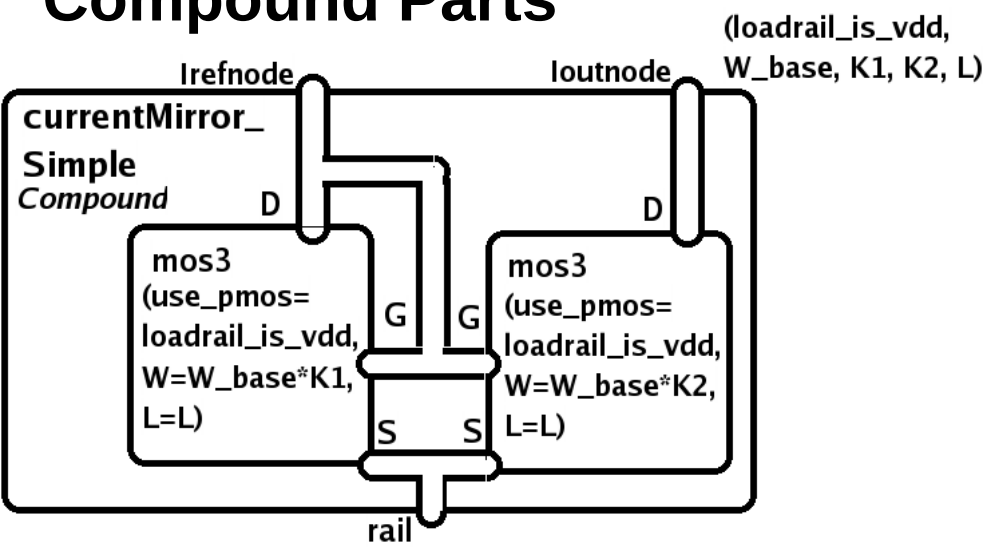


Types of Building Blocks in Library

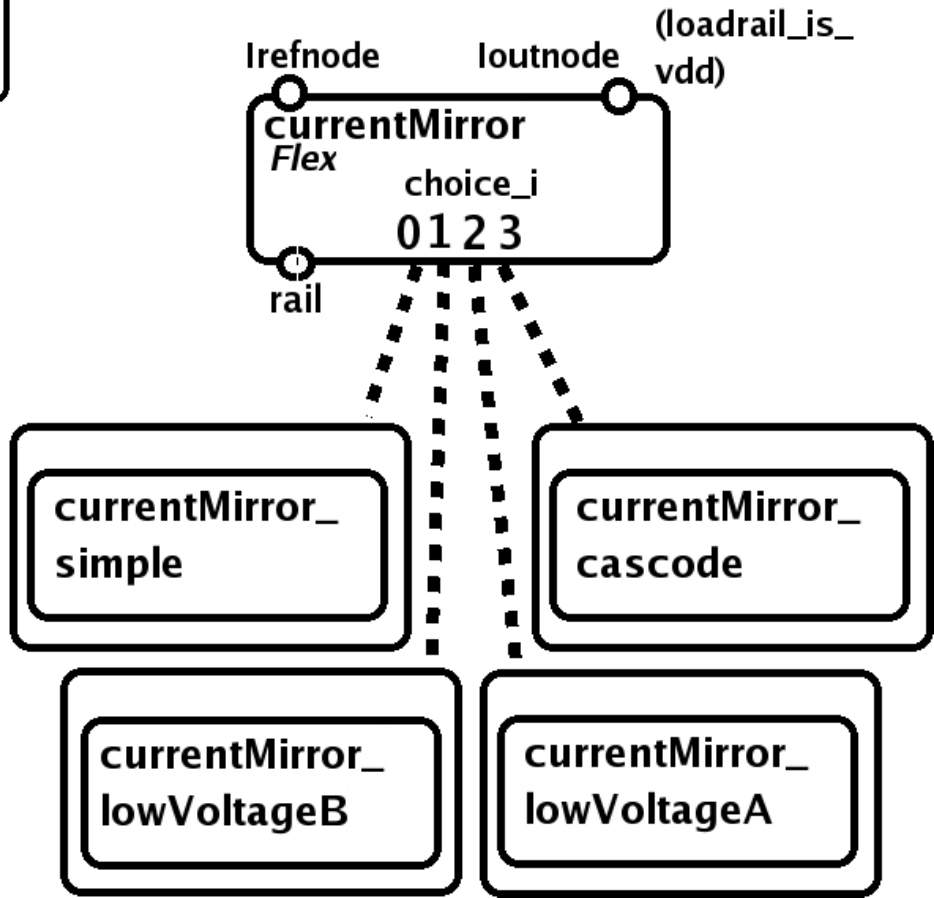
Atomic Parts



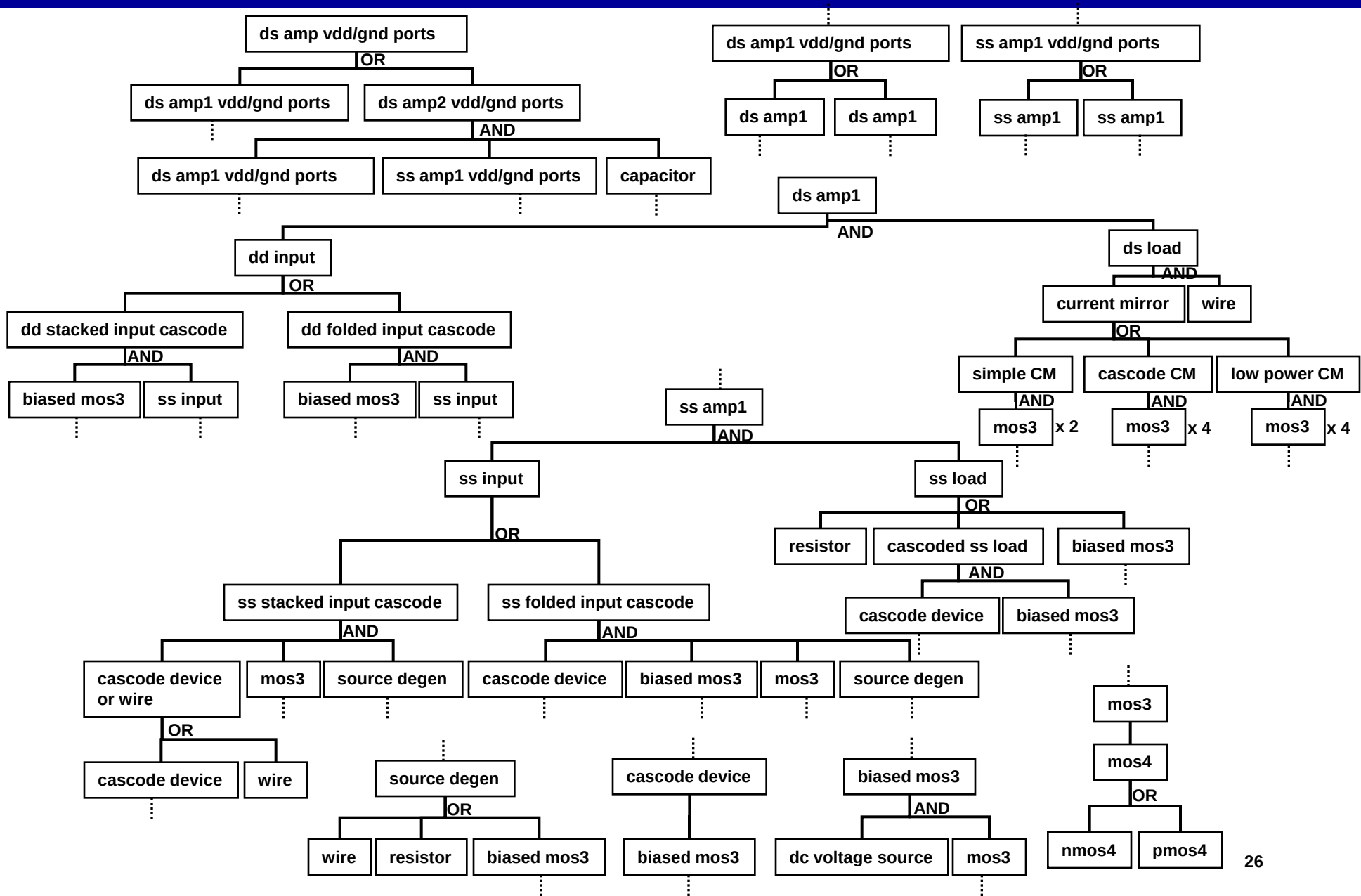
Compound Parts



Flexible Parts



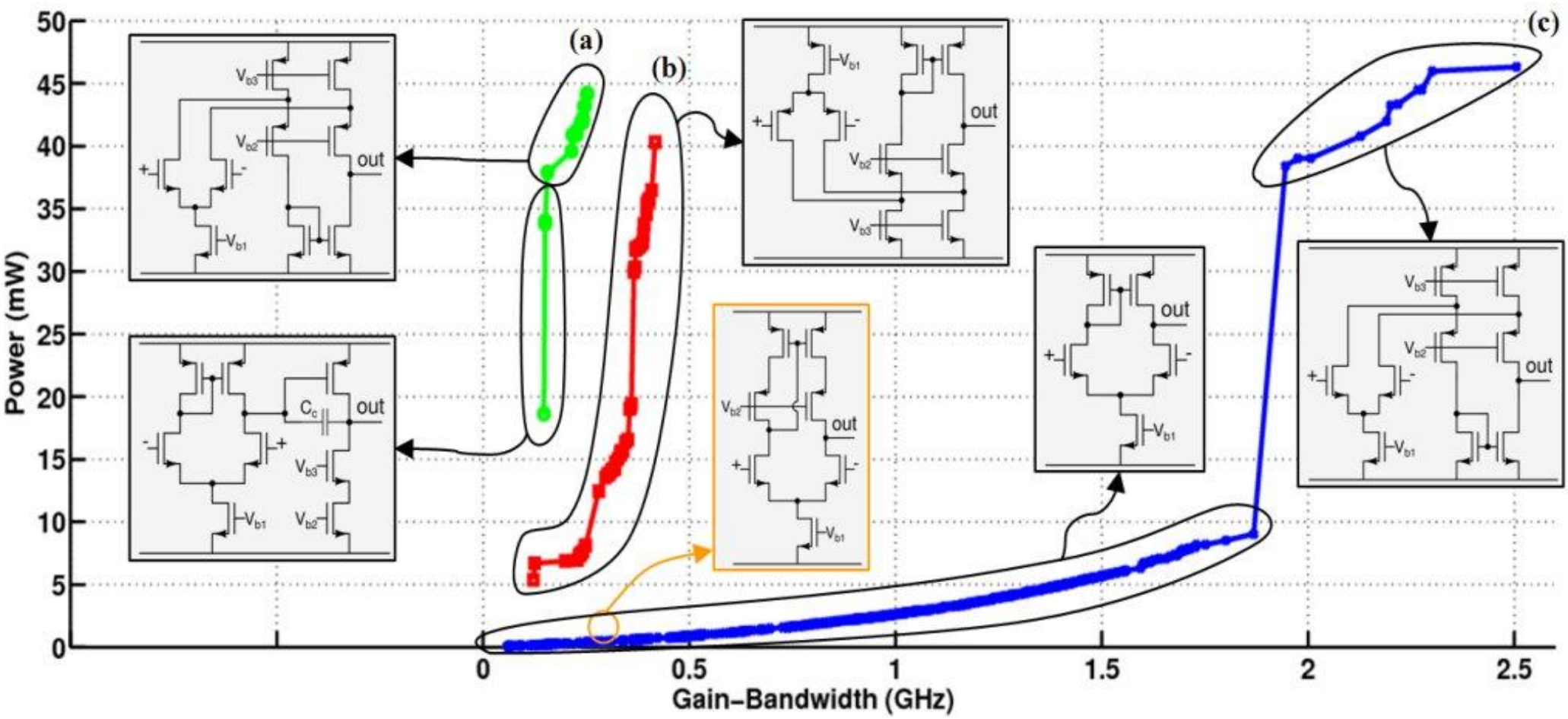
Whole BB library. 32 BBs → 3528 *trusted* topologies



How Rich is the Topology Space?

Technique (for opamps)	# Topologies	Trustworthy?
DARWIN [Kruiskamp et al 1995]	24	Yes
MINLP [Maulik et al 1995]	64	Yes
From-scratch GP [e.g. Koza 1996 – 2006]	>> billions	No
MOJITO	3528 (later, >100K)	Yes

Example Results: Hit Target Topologies on 3 Runs?



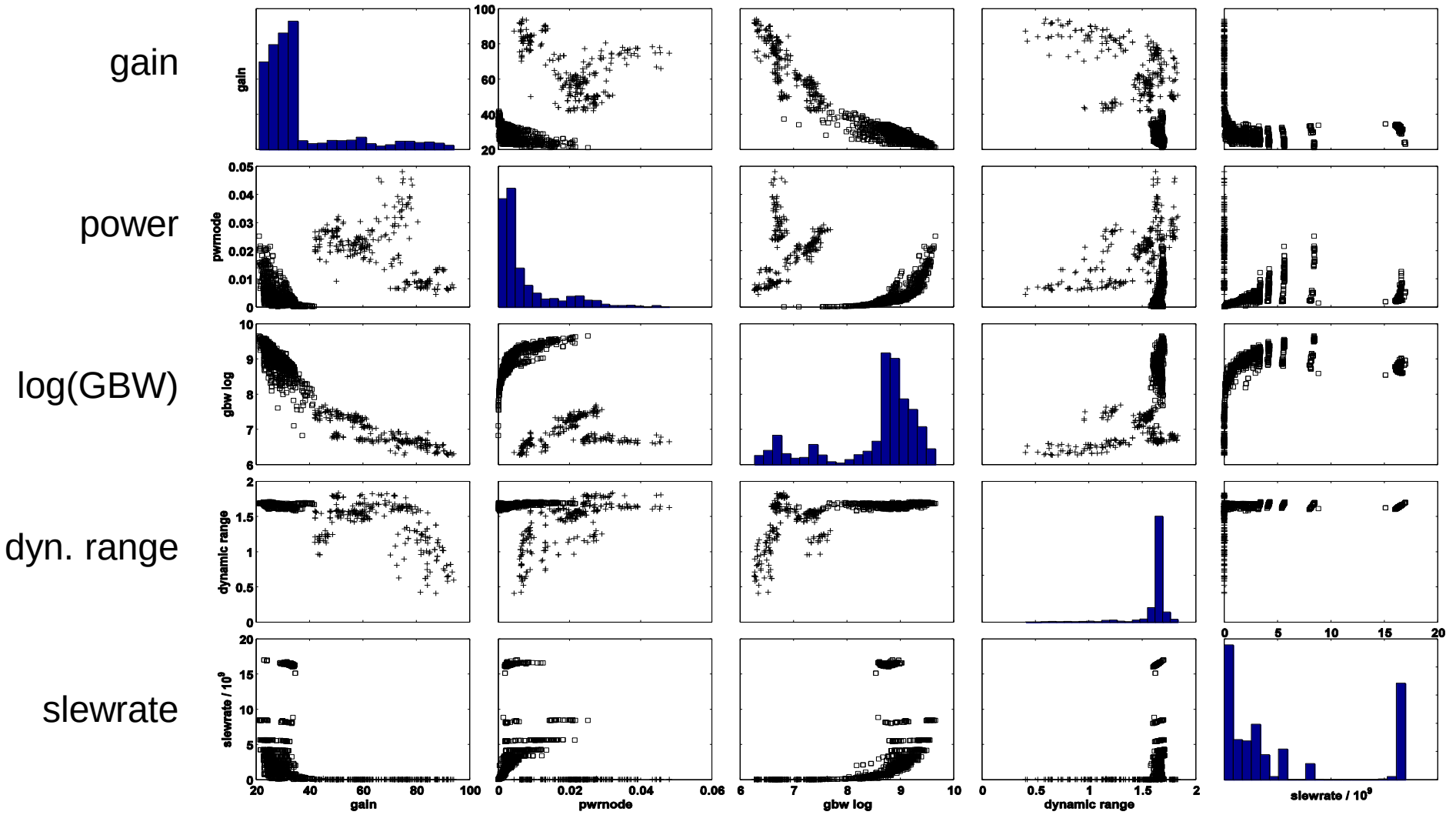
(a) $V_{cmm,in}$ = 1.5V => topologies need NMOS inputs (got them!)

(b) For $V_{cmm,in}$ = 0.3V => topologies need PMOS inputs (got them!)

(c) At $V_{cmm,in}$ = 0.9V, no restriction

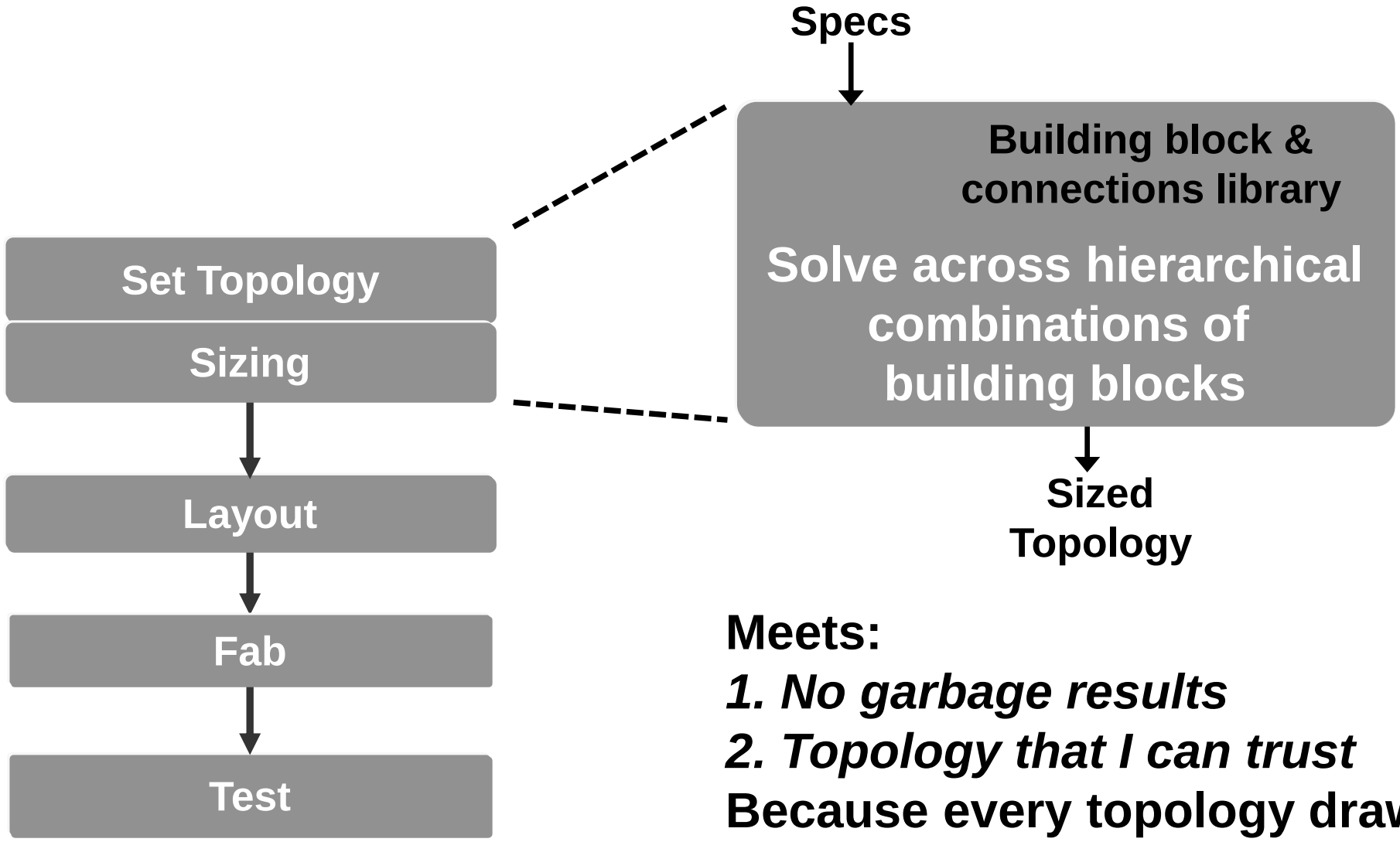
Overnight per run, 10 CPUs

Example Results: 5 Objectives (on dc, ac, tran)



- Runtime: Overnight on 30 CPUs
- Resulting tradeoffs DB with 1576 points, across 15 topologies
- Each "□" is a 1-stage opamp, and each "+" is a 2-stage opamp [Mcc GPTP 2008]

Rethinking Topology Synthesis, For Trust



Meets:

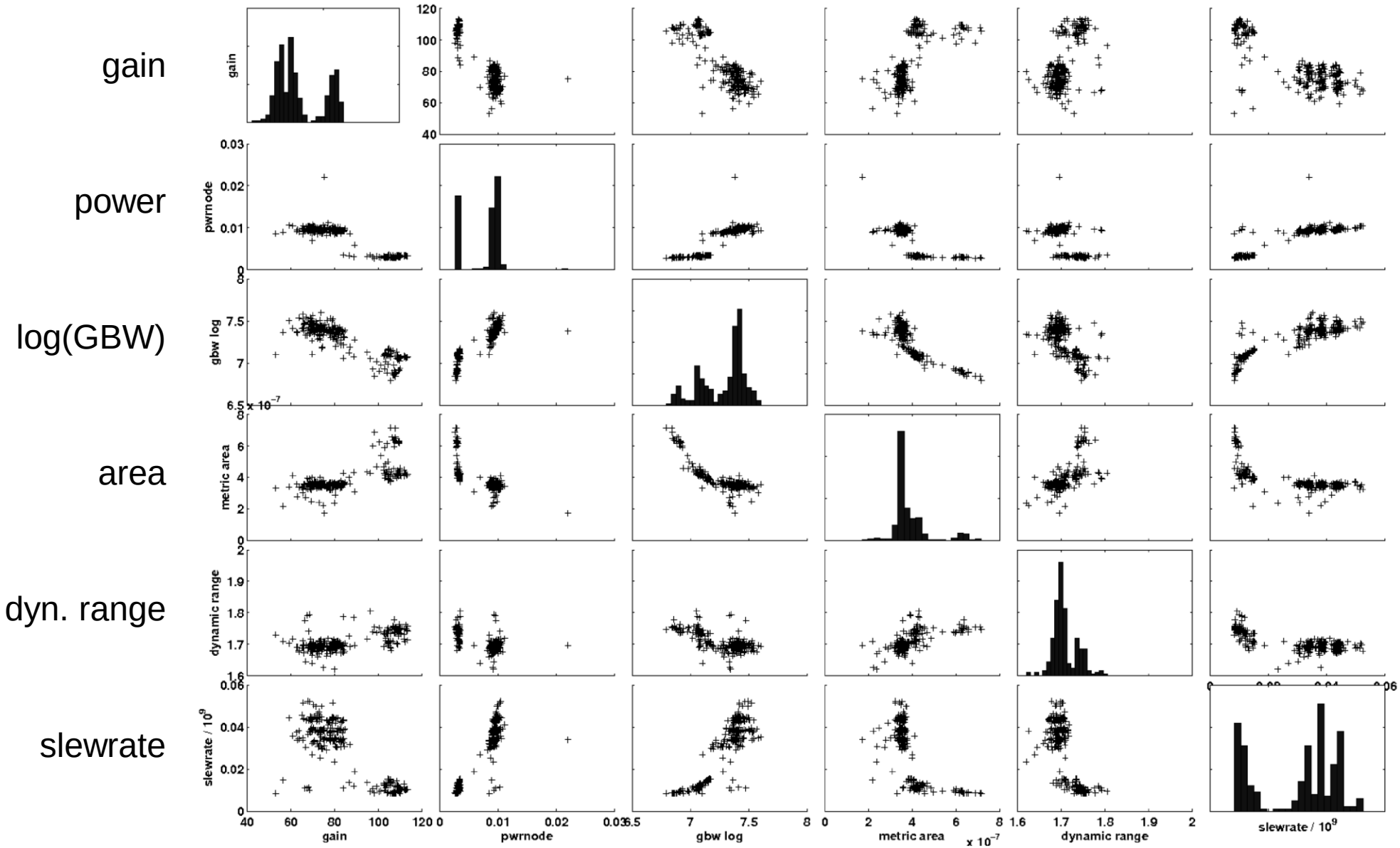
1. No garbage results

2. Topology that I can trust

Because every topology drawn from the set of topologies is trustworthy by construction

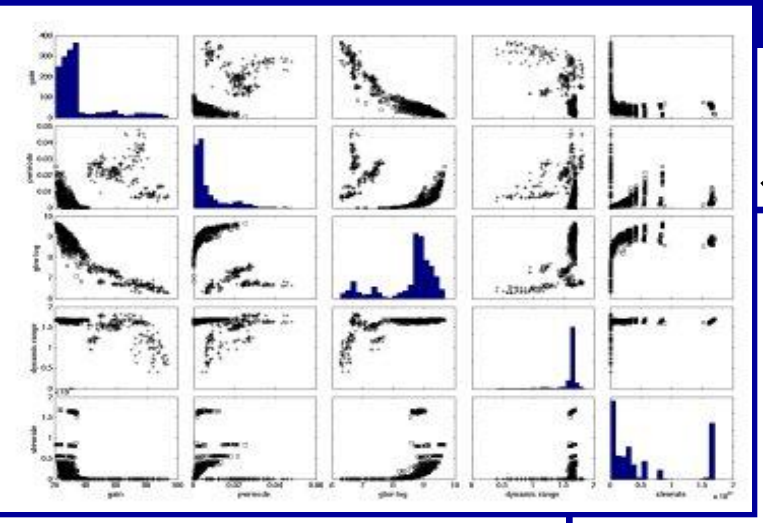
Once You Can Trust The Tool, You Can Go Meta!

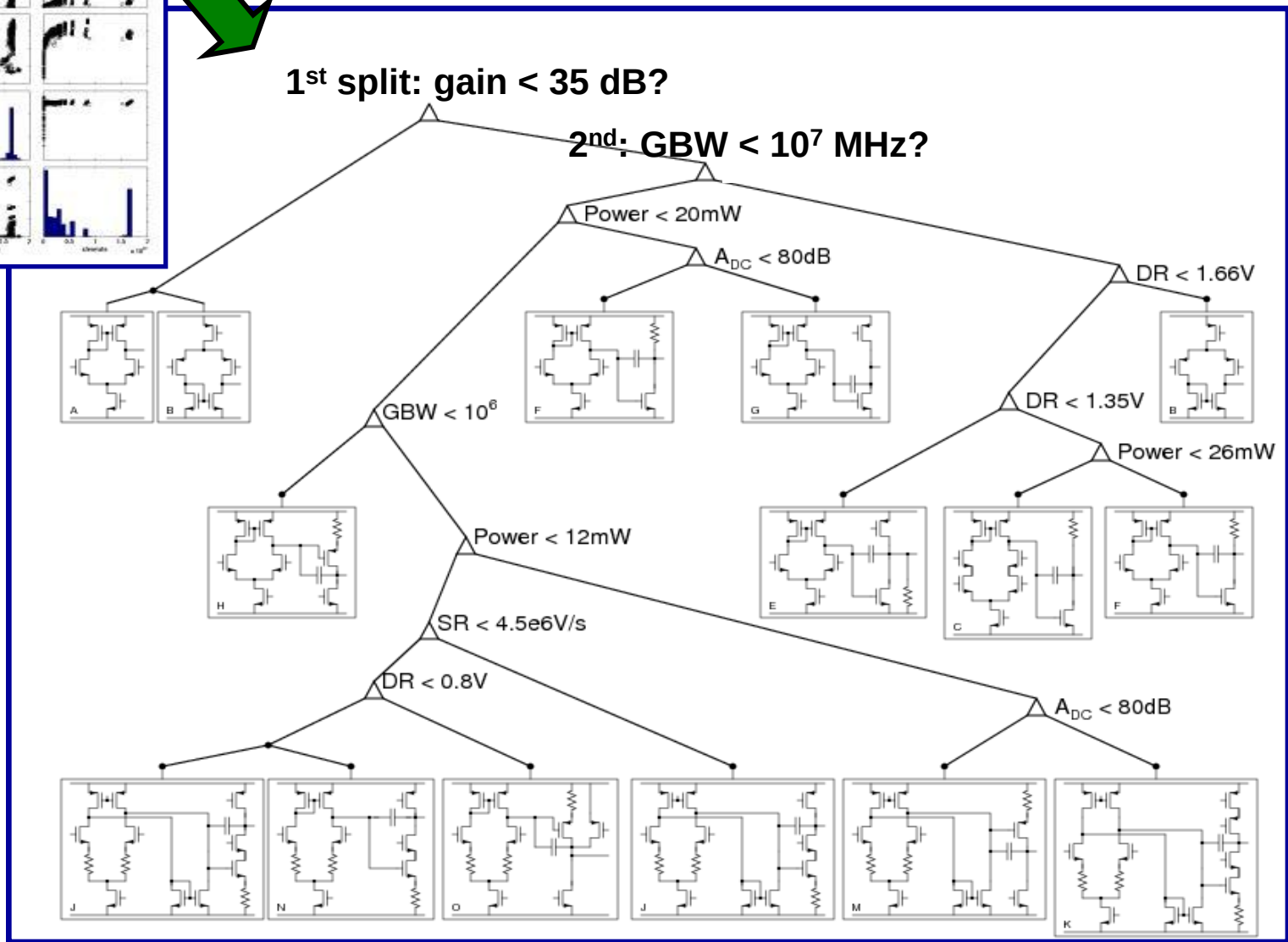
Example: Variation-Aware. Designs with >99% yield



Once You Can Trust The Tool, You Can Go Meta!

Example: Induce Decision Tree



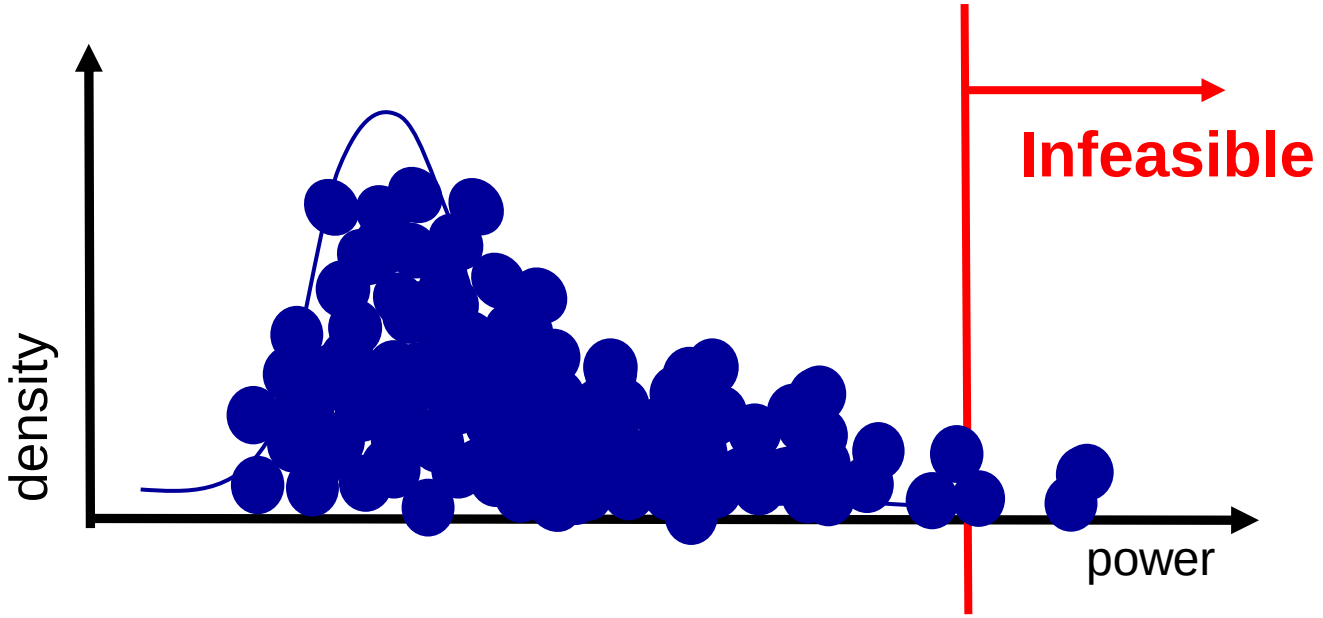


Outline: A Personal Story

- **Analog Topology Synthesis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**
- **High-Sigma Analysis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**

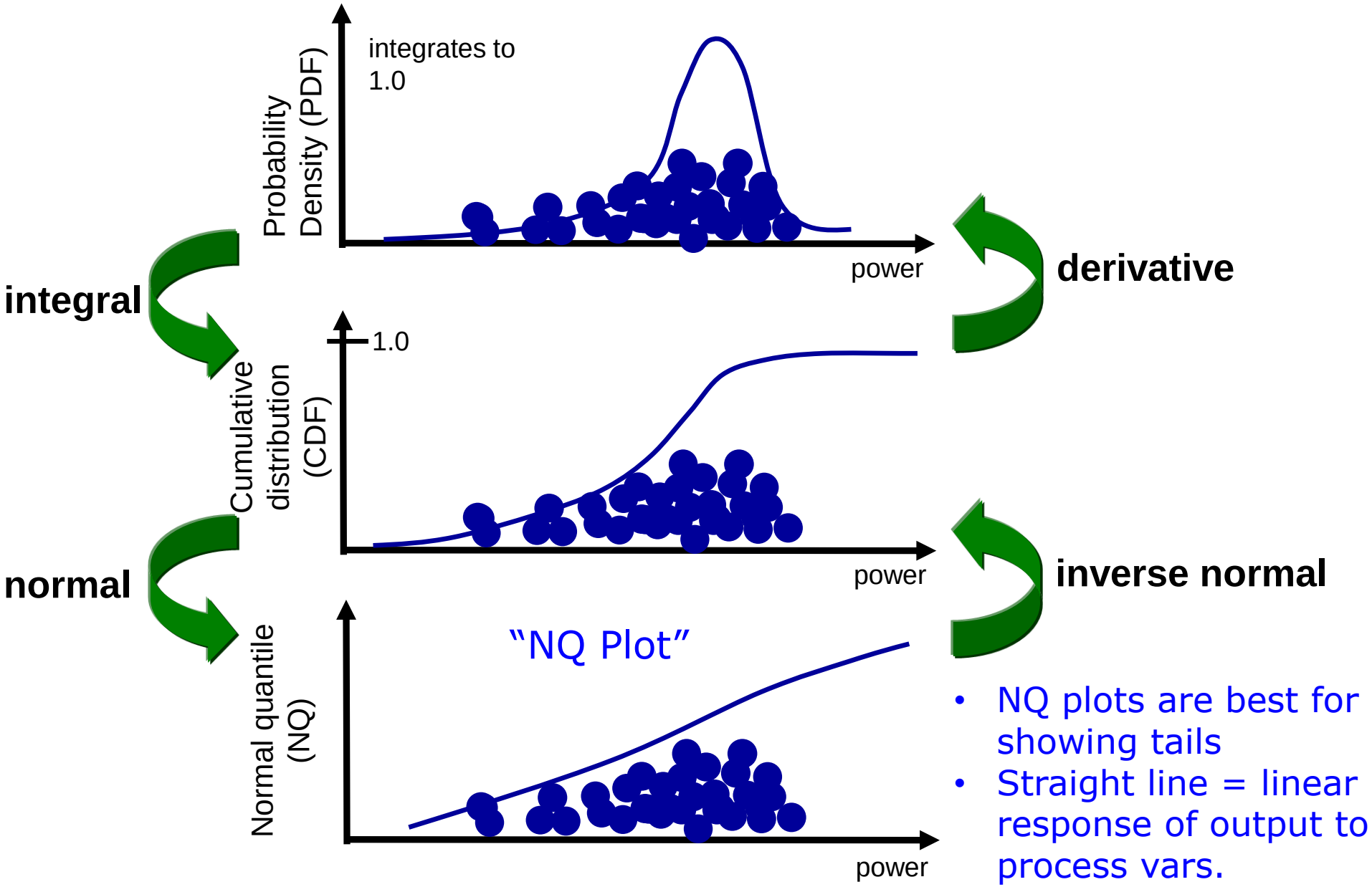
The Dream: “Monte Carlo” Style Results on 6σ Circuits? (More generally: rare event estimation)

5G MC samples



Getting a "Feel" for the Problem
Refresher: Visualizing Distributions – CDF and NQ

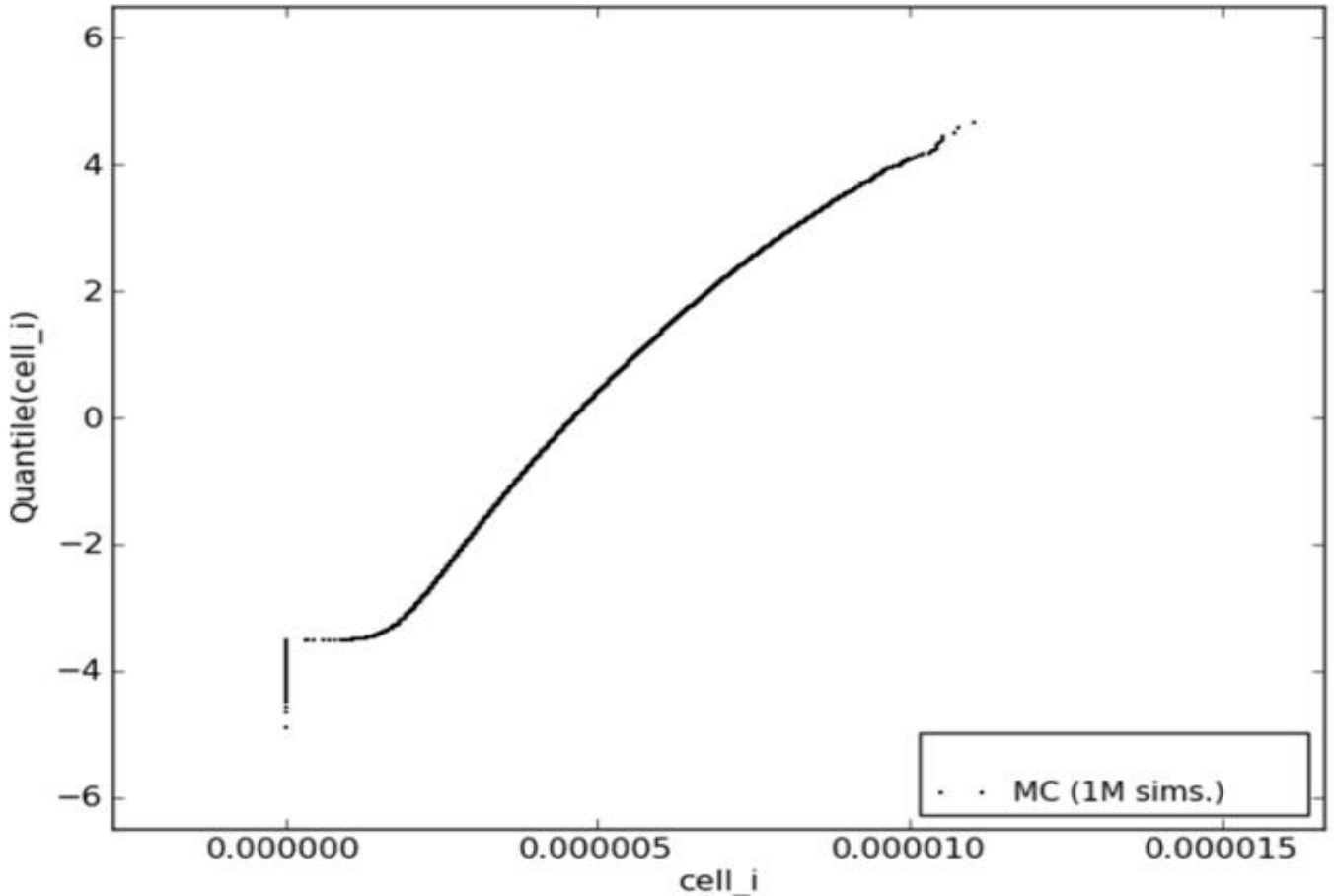
Three different views of the same distribution:



- NQ plots are best for showing tails
- Straight line = linear response of output to process vars.

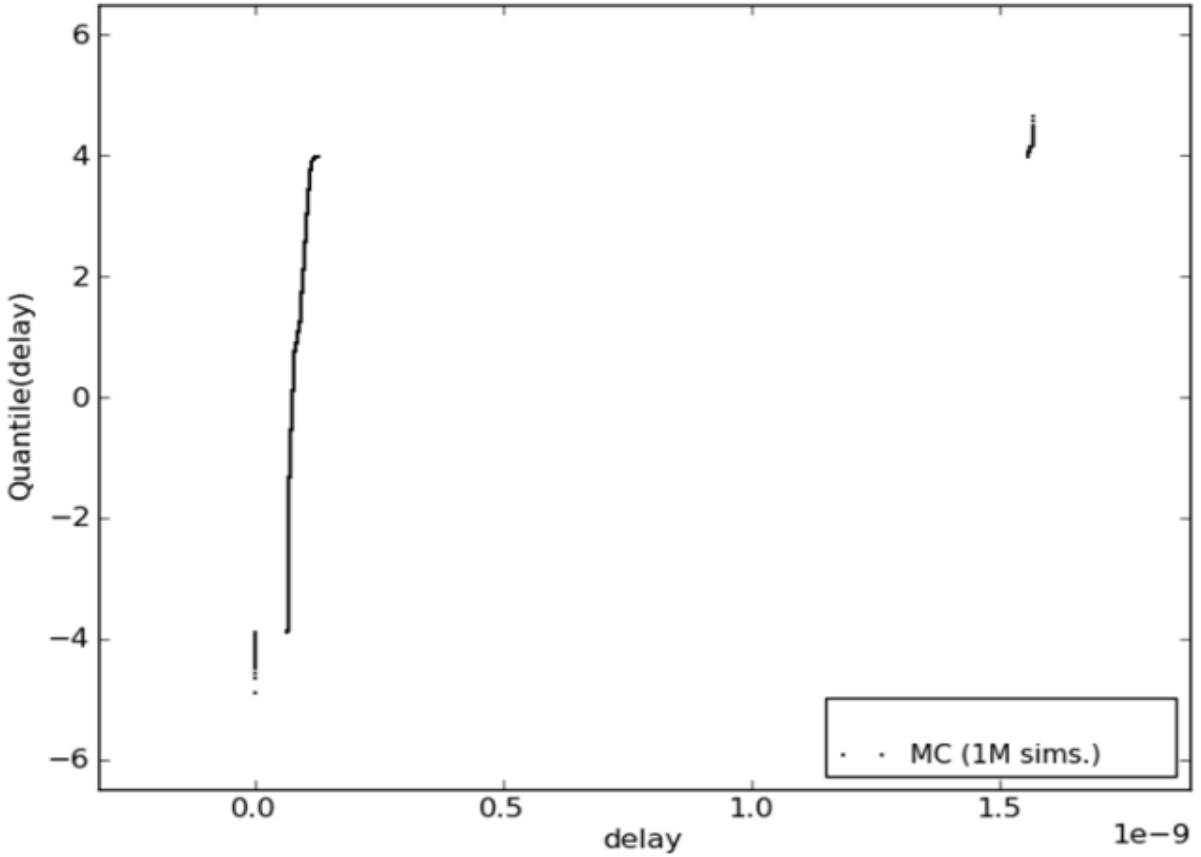
Getting a "Feel" for the Problem:
NQ Plot of Bitcell Read Current

- 6 devices x 10 local process variables / device = **60 variables**
- Simulated 1M MC samples. Each dot in curve is a sample.
  - The bend means quadratic response in that region
  - The dropoff / vertical means a flat response in that region (in this case, transistors turning off)

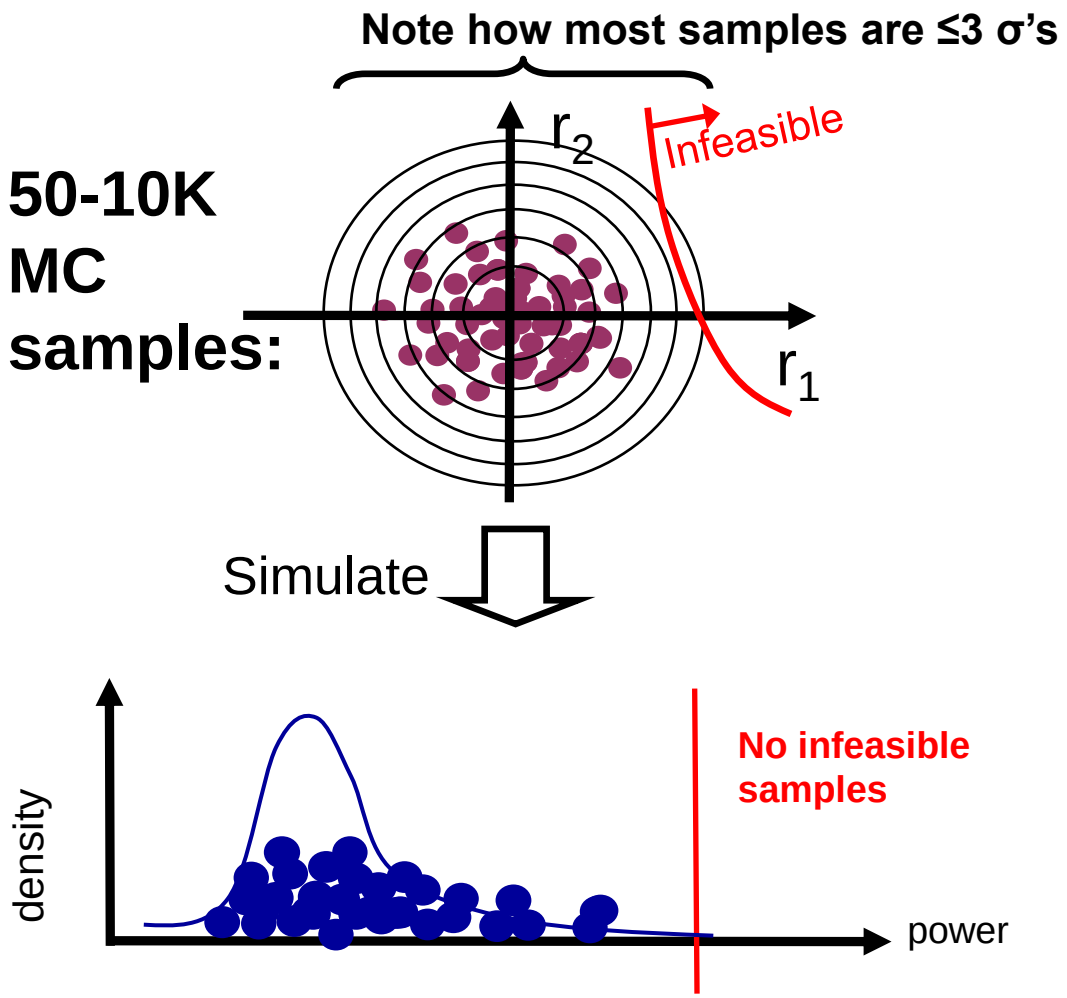


Getting a “Feel” for the Problem:
NQ Plot of Sense Amp Delay

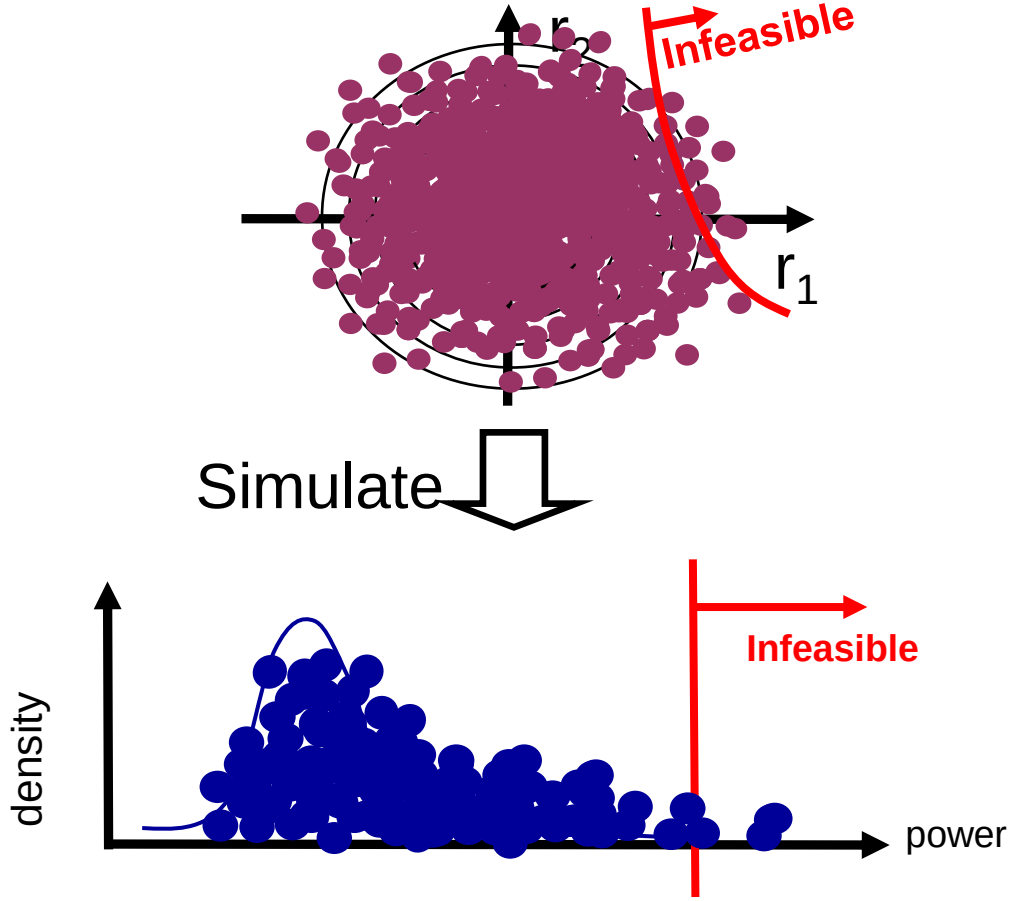
- 15 devices x 10 local process variables / device = 150 variables
- The three vertical “stripes” mean
  - three modes
  - tight distributions in each mode, almost flat response
  - left mode is “off”, right mode is “extreme”
  - gaps between stripes imply a discontinuity in response



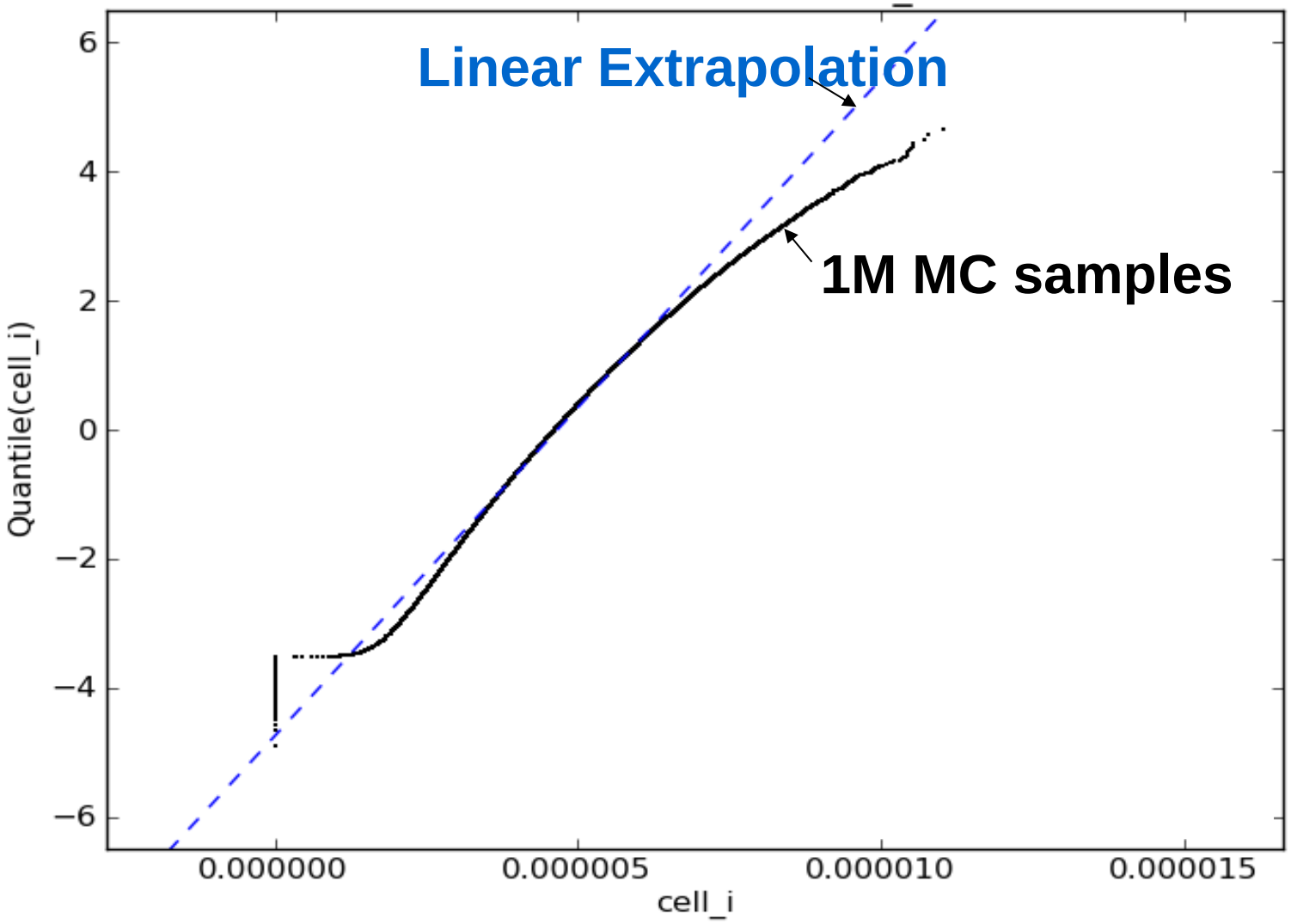
Approach: 10K MC Samples



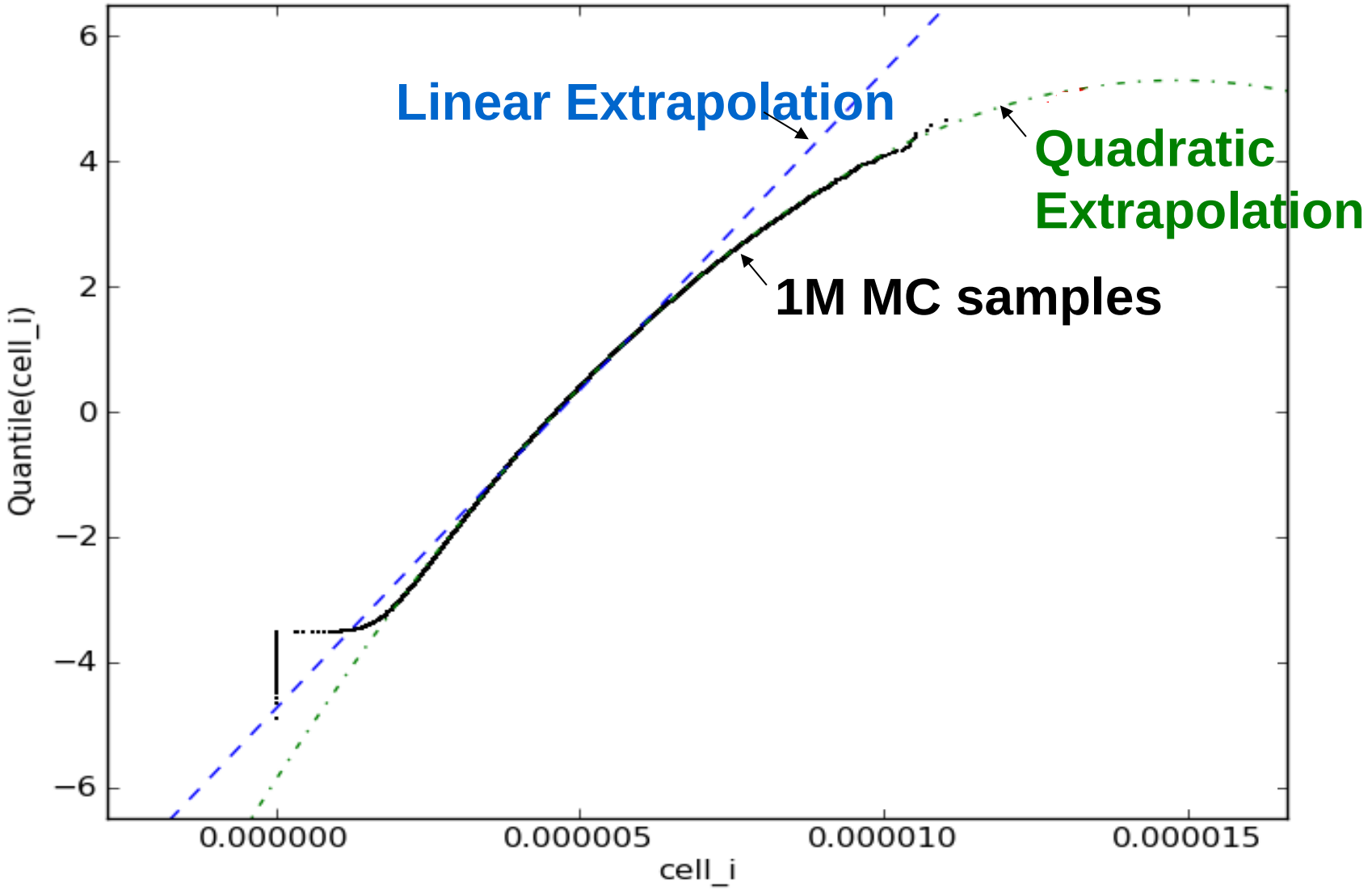
Approach: 5G MC Samples



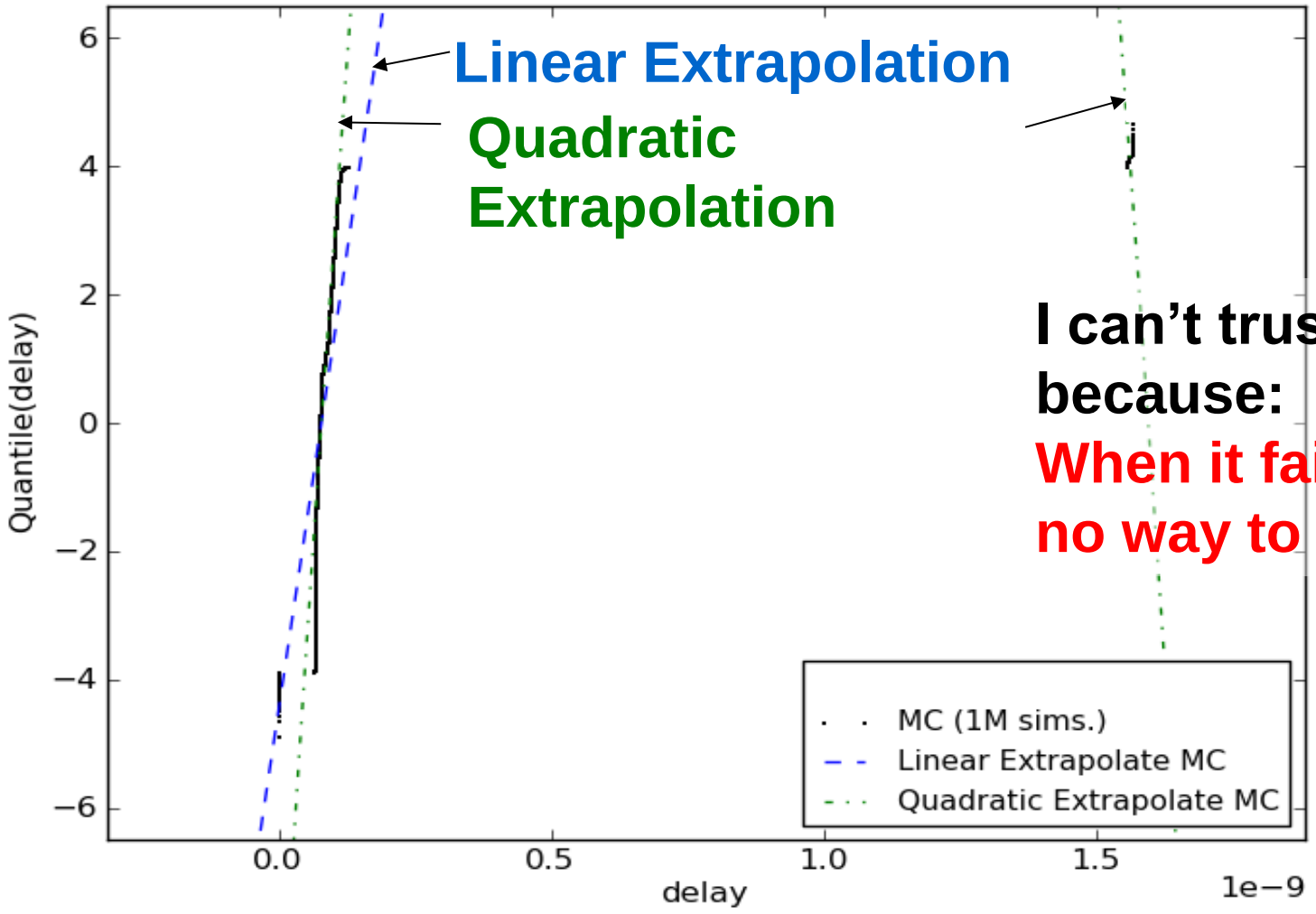
MC + Linear Extrapolation on Bitcell cell_i



MC + Quadratic Extrapolation on Bitcell cell_i



MC + Extrapolation on SA Delay

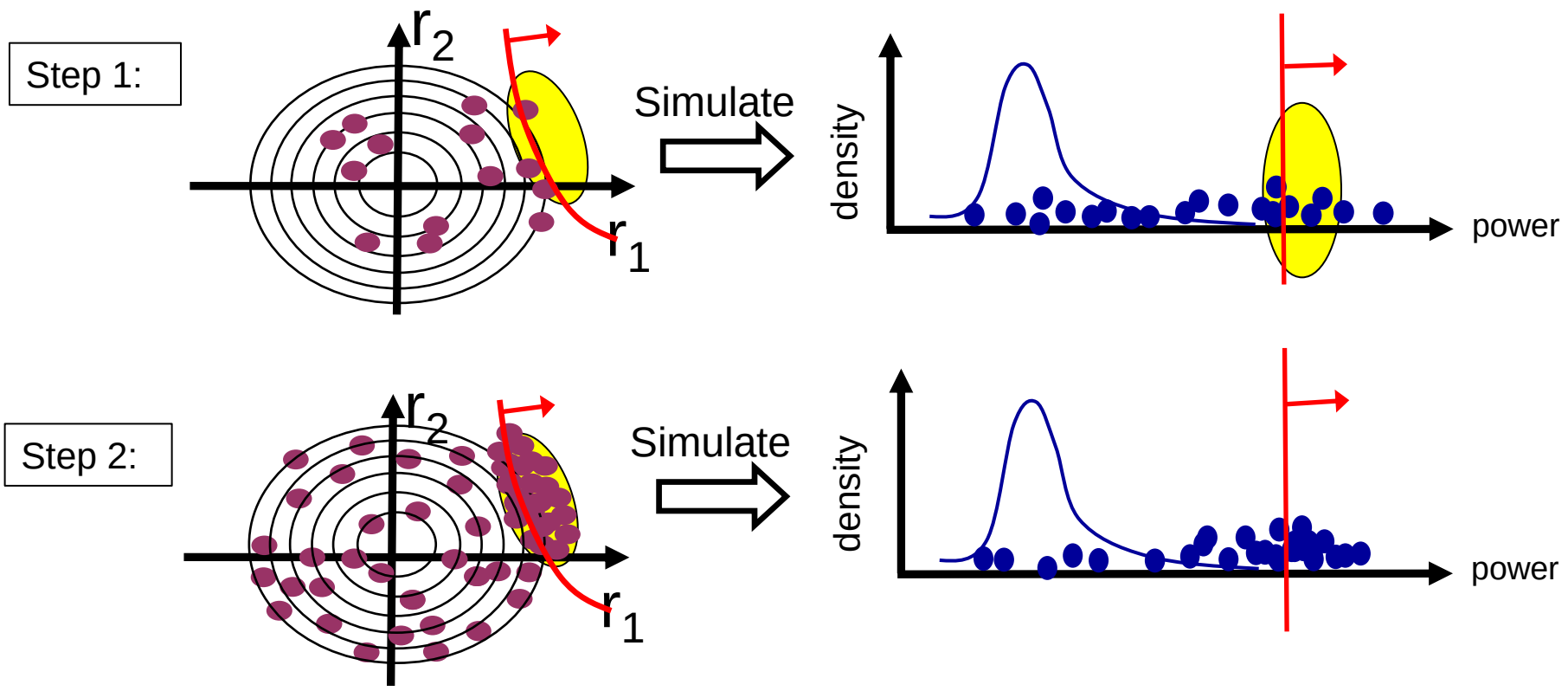


Outline: A Personal Story

- **Analog Topology Synthesis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**
- **High-Sigma Analysis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**

The First Cut: Importance Sampling

1. Find highest-probability regions of process space that cause infeas.
   - E.g. Draw uniformly-distributed samples
   - E.g. Treat as optimization problem: “maximize prob s.t. infeas.”
2. Draw & simulate points from a distribution *biased to those regions*
3. When estimating yield, weight samples



Outline: A Personal Story

- **Analog Topology Synthesis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**
- **High-Sigma Analysis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**

My experience

Solido: Wanna buy our IS-based high-sigma tool?

Customer: how can I trust it?

Solido: Uhhh… faith?

Customer: <click>

My experience 2/2

Solido: Wanna try our IS-based high-sigma tool?

Customer: OK, let's try.

Solido: <installs software>

Customer: <tries software>. Pfail = 1e-40. Huh?

Solido: Odd, IS [defensive sampling] theory says it should converge…

Customer: <click>

My experience 2/2

Solido: Wanna try our IS-based high-sigma tool?

Customer: OK, let's try.

Solido: <installs software>

Customer: <tries software>. Pfail = 1e-40. Huh?

Solido: Odd, IS [defensive sampling] theory says it should converge…

Customer: <click>

Solido: <stops shipping IS tool>

Importance Sampling: Main Challenge

Need to find the most probable regions that are infeasible

- If regions are missed, then yield is too optimistic
- If just 1 region: ≈a global optimization problem, with exponential complexity in # process variables. 10^{150}
- If >1 region, it's even harder

Hard to trust because:

When it fails, I have no way to tell

Outline: A Personal Story

- **Analog Topology Synthesis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**
- **High-Sigma Analysis**
  - **The dream**
  - **The first cut**
  - **The pain**
  - **Rethinking wrt trust**

Rethinking the problem

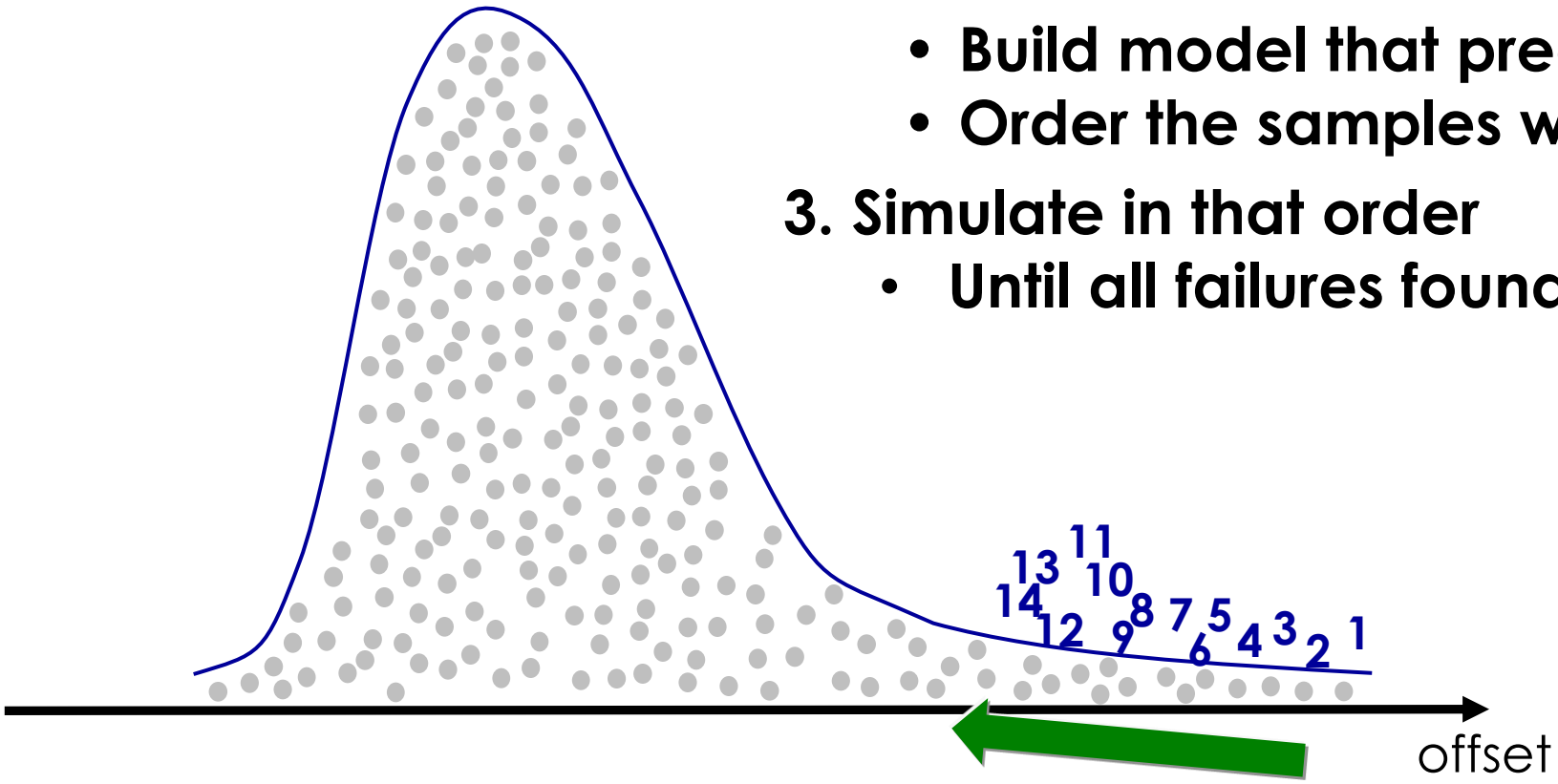
Hint: Benefit of MC : complexity independent of dimensionality

Hint: In topology synthesis, we simplified the problem by adding more information about the problem (analog BBs)

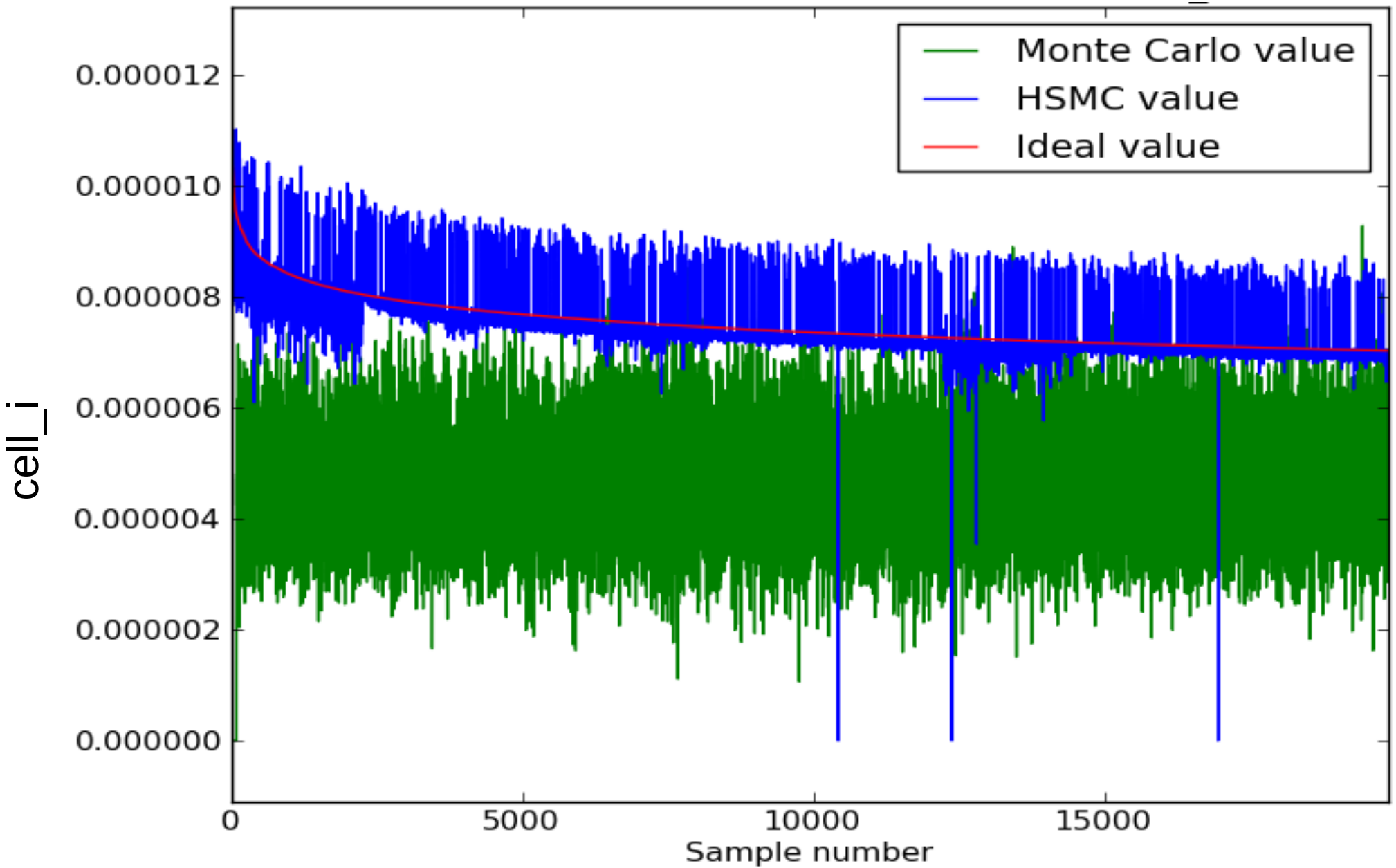
Hint: Saying "problem is 6 sigma" is (just) 10^{10} MC samples. $10^{10} \ll 10^{150}$

High-Sigma Monte Carlo Algorithm (HSMC)

1. Generate (but don't simulate) 5G Monte Carlo samples
2. Order the 5G samples:
   - Choose initial samples, & simulate
   - Build model that predicts order
   - Order the samples with model
3. Simulate in that order
   - Until all failures found

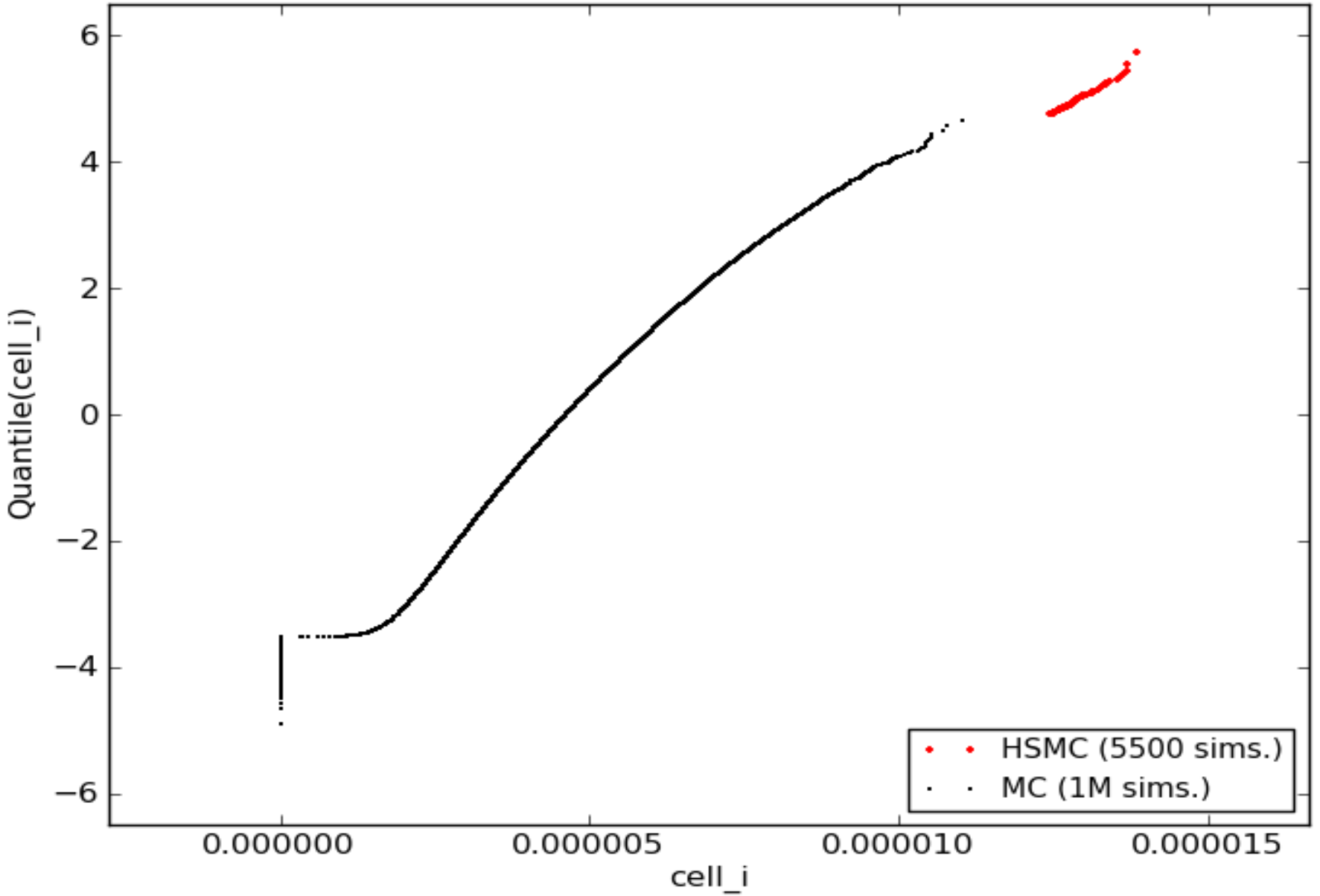


HSMC Convergence on Bitcell cell_i

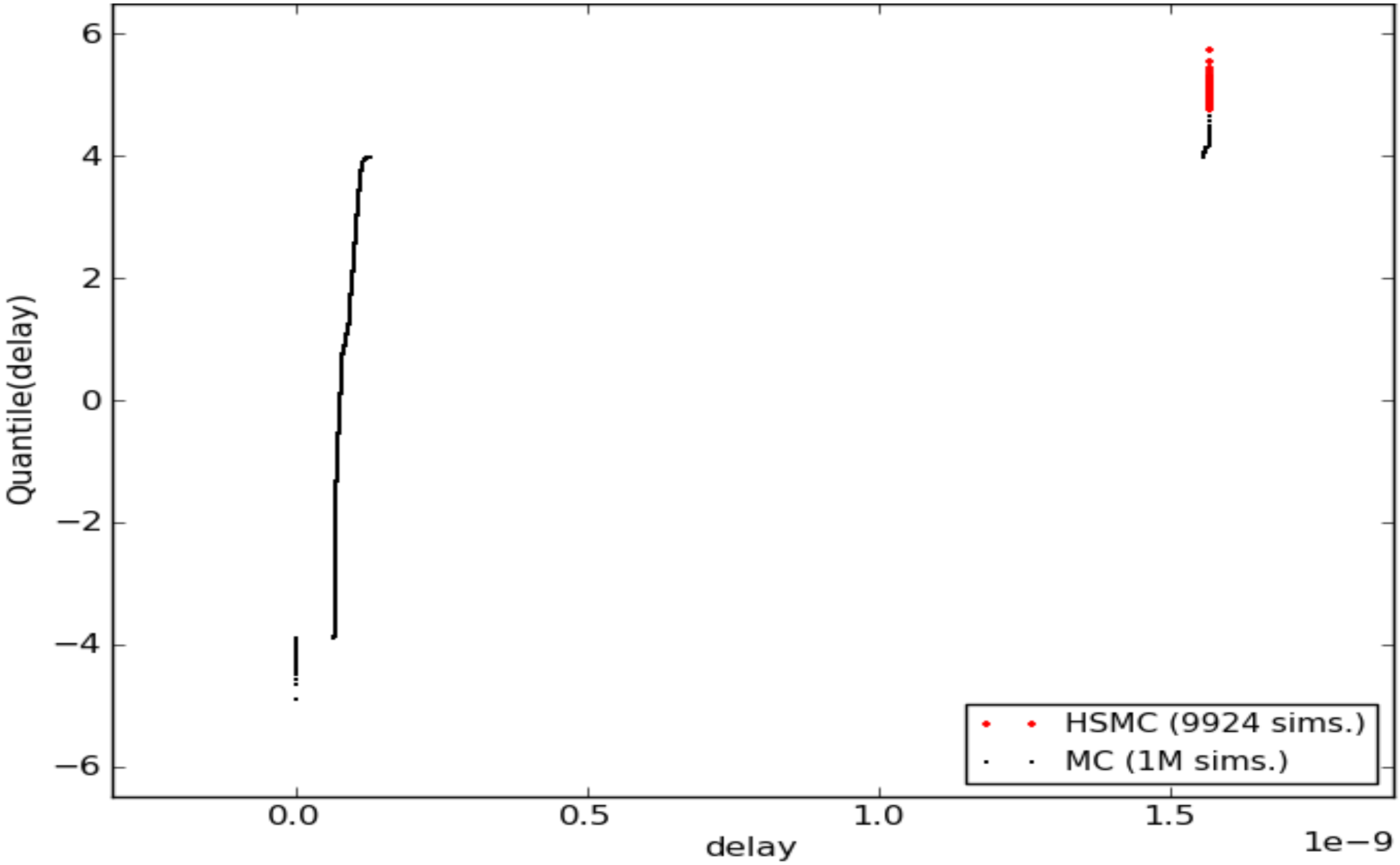


NQ Plot of Bitcell cell_i

(HSMC worked off 100M generated)

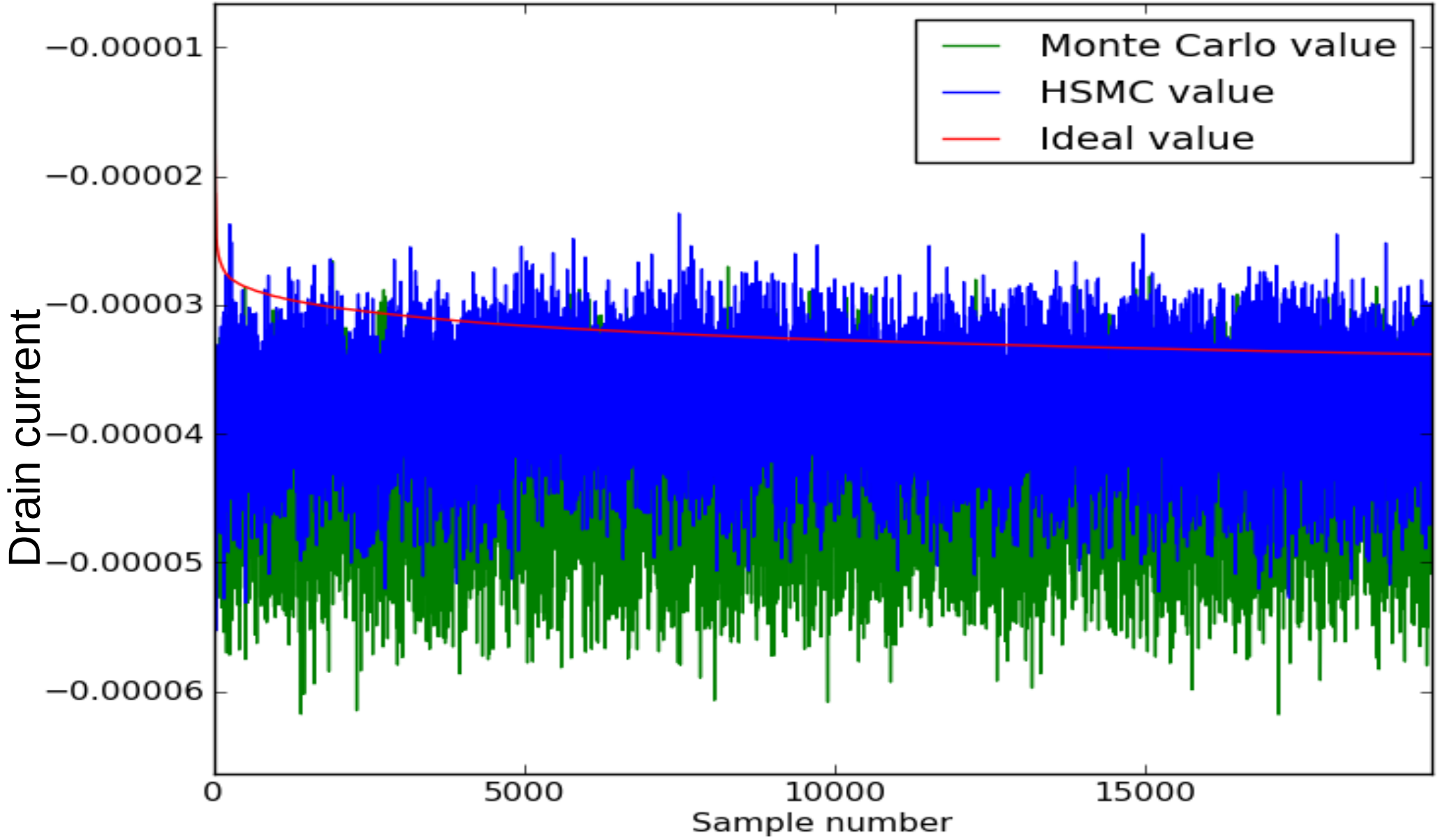


NQ Plot of Sense Amp Delay



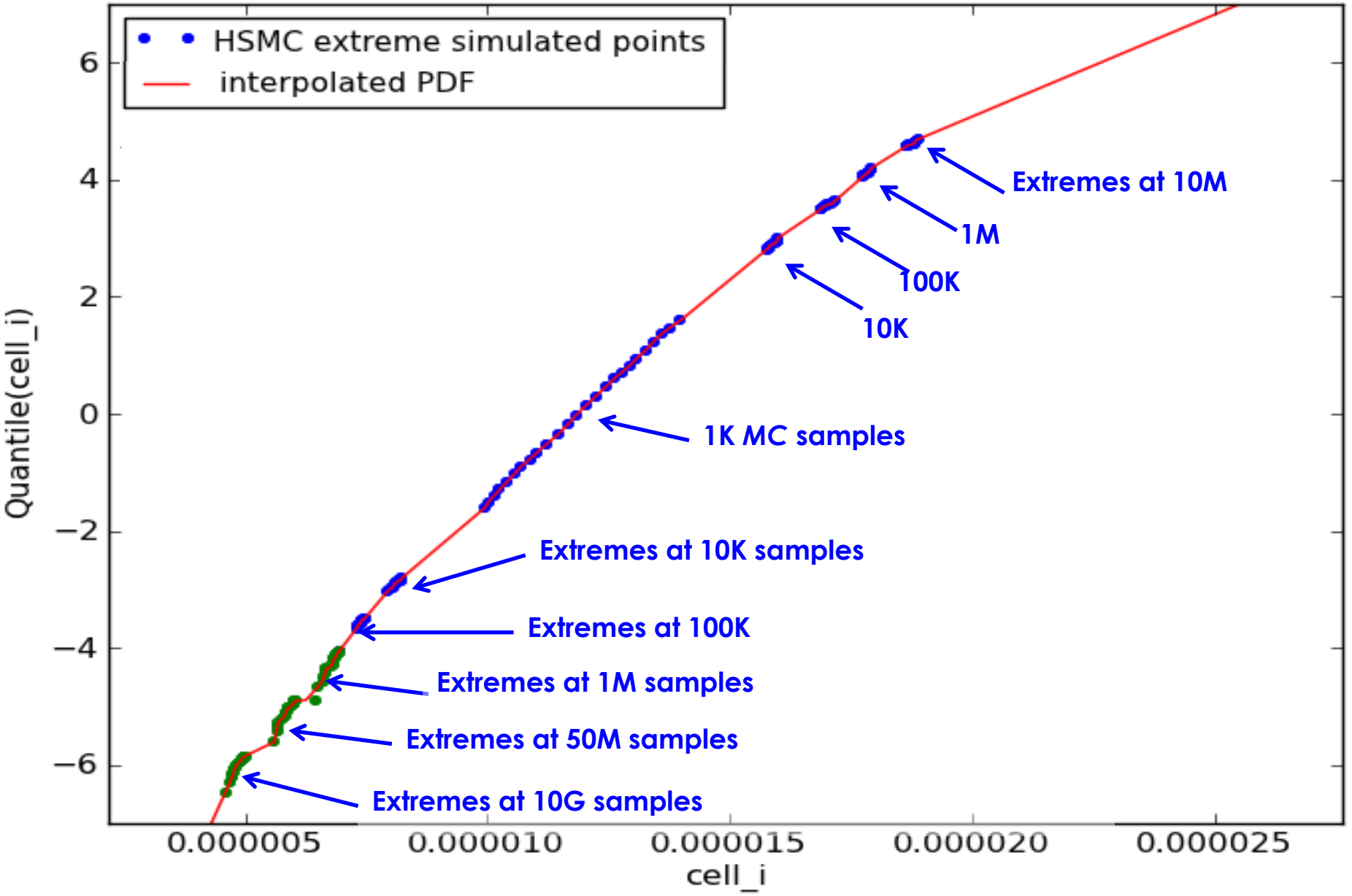
Q: If it fails, how can I tell? A: poor or no trend

Example: flip flop drain current. (Vdd was too low.)

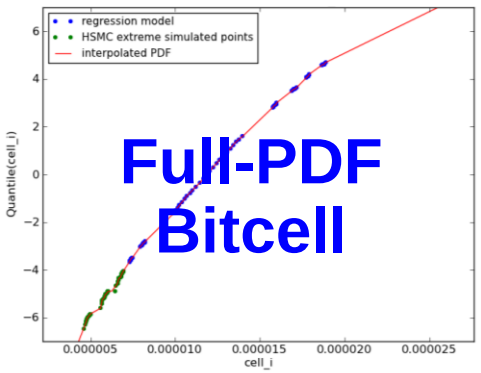


Once You Trust The Tool, You Can Go Meta

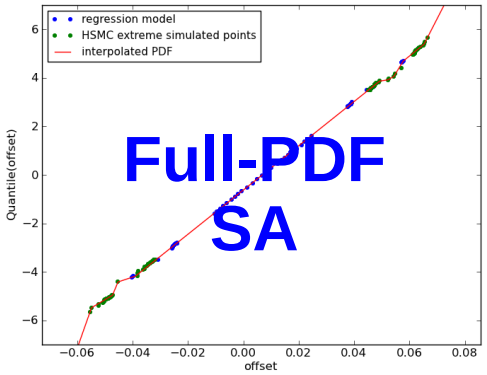
Example: Full PDF Extraction



Once You Trust The Tool, You Can Go Meta
Example: Array-Level Memory Analysis



Full-PDF Bitcell



Full-PDF SA

Nested MC on PDFs

Summary Table

(With N_SA = 256, N_BIT = 1K, C = 5.000f)

Probe time T	Column yield	[Column lower, Upper]	System yield
600.0ps	0.02000%	[0.005485%, 0.07290%]	0.0%
700.0ps	0.07000%	[0.03391%, 0.1444%]	0.0%
800.0ps	0.2700%	[0.1856%, 0.3926%]	0.0%
900.0ps	[illegible]	[illegible]	0.0%
1.000ns	7.55%	[7.0483%, 8.0842%]	5.681e-286%
1.100ns	22.3%	[21.494%, 23.126%]	1.466e-165%
1.200ns	49.27%	[illegible]	2.000e-77%
1.300ns	75.55%	[74.697%, 76.382%]	6.730e-30%
1.400ns	91.64%	[91.081%, 92.166%]	1.967e-8%
1.500ns	97.88%	[97.578%, 98.144%]	0.4146%
1.600ns	99.520%	[99.364%, 99.638%]	29.177%
1.700ns	99.9300%	[99.856%, 99.9661%]	83.588%
1.800ns	99.99%	[99.9434%, 99.99823%]	97.472%

Array-Level Yield Vs. Performance

Trust in Other CAD problem domains?

Domain	Less Trust	More trust
Topology synthesis	Open-ended	Trustworthy-by-construction
High-sigma analysis	MC + Extrapolation, IS	High-sigma MC
Dynamic circuit analysis	Hand equations, Symbolic analysis	SPICE (solved KCL?), fSPICE (SAT solved?)
Large-scale dynamic circuit analysis	Behavioral modeling, FastSPICE (approx. MOS models)	Analog FastSPICE
PVT Analysis	Sensitivity-based, sweep-based	Fast PVT (global worst-case opt.)
3-sigma analysis	Sensitivity-based	MC

“All you need is a little faith, trust and pixie dust”

-Peter Pan (J.M. Barrie)

“I need trust”

-Any sane designer

Conclusion

- **Analog Topology Synthesis**
  - **Dream, first cut, pain, rethink**
- **High-Sigma Analysis**
  - **Dream, first cut, pain, rethink**
- ***Trust matters!***